GD25Q512MC

DATASHEET

Contents

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  - -64M-byte
  - -256 bytes per programmable page
- Standard, Dual, Quad SPI
  - -Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#/ RESET#
  - -Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#/ RESET#
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  - -3 or 4-Byte Addressing Mode
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    - Dual I/O Data transfer up to 208Mbits/s
    - Quad I/O Data transfer up to 416Mbits/s
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- Package Information
  - -SOP16 (300mil)
  - -WSON8 (6*8mm)
  - -TFBGA-24(5*5 ball array)
  - -TFBGA-24(6*4 ball array)

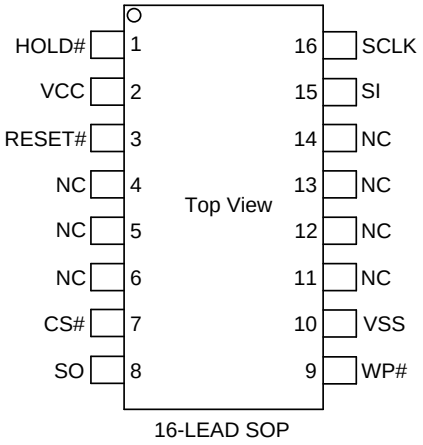
Note: 1.Please contact GigaDevice for details.

2. GENERAL DESCRIPTION

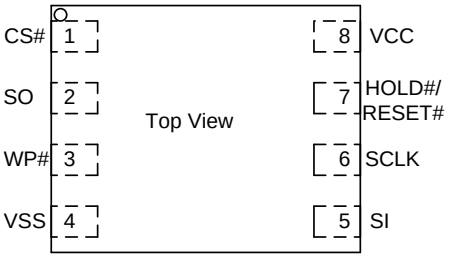
The GD25Q512MC (512M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), and I/O3 (HOLD#/ RESET#). The Dual I/O data is transferred with speed of 208Mbits/s and the Quad I/O & Quad output data is transferred with speed of 320Mbits/s.

CONNECTION DIAGRAM

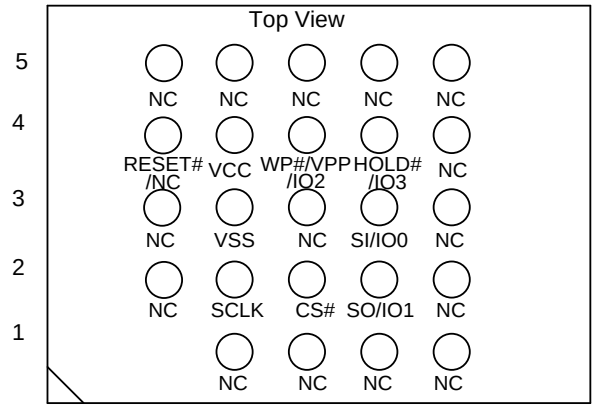
Figure 1 Connection Diagram



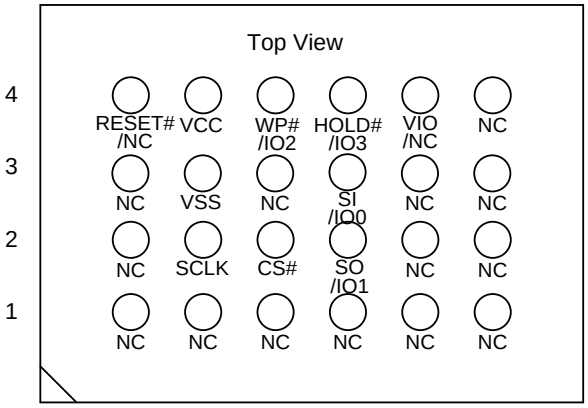
16-LEAD SOP



8 - LEAD WSON



24-BALL TFBGA (5x5 ball array)



24-BALL TFBGA (6x4 ball array)

PIN DESCRIPTION

Table 1 Pin Description for WSON8 package

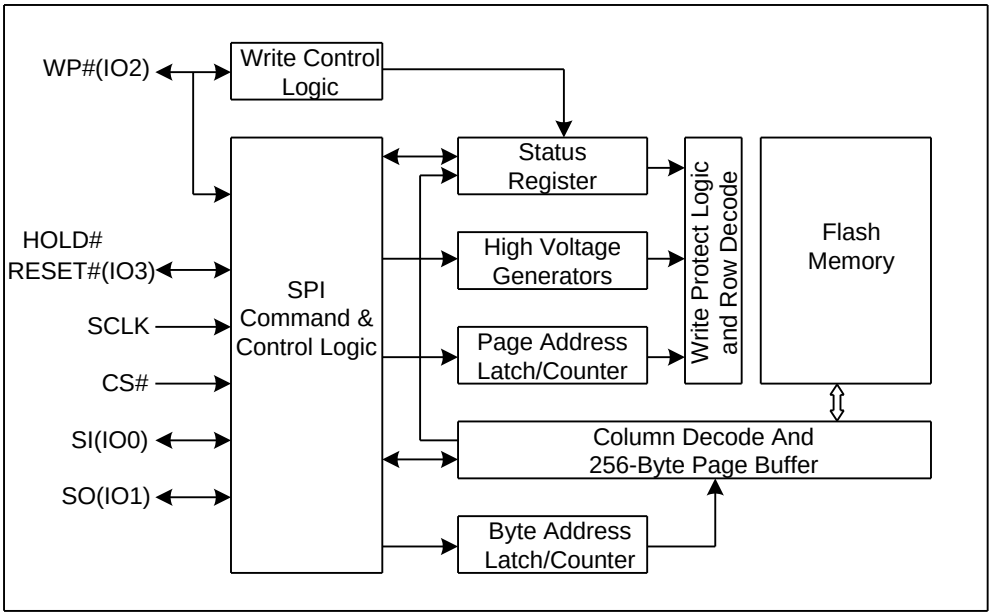
Pin Name	I/O	Description
CS#	**I**	Chip Select Input
SO (IO1)	**I/O**	Data Output (Data Input Output 1)
WP# (IO2)	**I/O**	Write Protect Input (Data Input Output 2)
VSS		Ground
SI (IO0)	**I/O**	Data Input (Data Input Output 0)
SCLK	**I**	Serial Clock Input
HOLD#/RESET# (IO3)	**I/O**	Hold or Reset Input (Data Input Output 3)
VCC		Power Supply

Table 2 Pin Description for SOP16 package and TFBGA24 package

Pin Name	I/O	Description
CS#	**I**	Chip Select Input
SO (IO1)	**I/O**	Data Output (Data Input Output 1)
WP# (IO2)	**I/O**	Write Protect Input (Data Input Output 2)
VSS		Ground
SI (IO0)	**I/O**	Data Input (Data Input Output 0)
SCLK	**I**	Serial Clock Input
HOLD#/(IO3)	**I/O**	Hold Input (Data Input Output 3)
RESET#	**I**	Reset Input
VCC		Power Supply

BLOCK DIAGRAM

Figure 2 Block Diagram



3. MEMORY ORGANIZATION

GD25Q512MC

Table 3 GD25Q512MC Memory Organization

Each device has	Each block has	Each sector has	Each page has	
64M	64/32K	4K	256	bytes
256K	256/128	16	-	pages
16384	16/8	-	-	sectors
1024/2048	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE

GD25Q512MC

Table 4 GD25Q512MC 64K Bytes Block Sector Architecture

Block	Sector	Address range		Advanced Block Protection unit
1023	16383	03FF F000H	03FF FFFFH	4KB
	……	……	……	……
	16368	03FF 0000H	03FF 0FFFH	4KB
1022	16367	03FE F000H	03FE FFFFH	64KB
	……	……	……	
	16352	03FE 0000H	03FE 0FFFH	
1021	16351	03FD F000H	03FD FFFFH	64KB
	……	……	……	
	16336	03FD 0000H	03FD 0FFFH	
……	……	……	……	……
	……	……	……	
	……	……	……	
……	……	……	……	
	……	……	……	
	……	……	……	
2	47	0002 F000H	0002 FFFFH	64KB
	……	……	……	
	32	0002 0000H	0002 0FFFH	
1	31	0001 F000H	0001 FFFFH	64KB
	……	……	……	
	16	0001 0000H	0001 0FFFH	
0	15	0000 F000H	0000 FFFFH	4KB
	……	……	……	……
	0	0000 0000H	0000 0FFFH	4KB

Note:

1. Advanced Block Protection unit for block 1023 and block 0 is 4KB sector, while unit for block 1 to block 1022 is 64KB blocks (512Kbit).

4. DEVICE OPERATION

SPI Mode

Standard SPI

The GD25Q512MC features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The GD25Q512MC supports Dual SPI operation when using the “Dual Output Fast Read”, “Dual Output Fast Read with 4-byte address”, “Dual I/O Fast Read” and “Dual I/O Fast Read with 4-byte address” commands (3BH 3CH BBH and BCH). These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI

The GD25Q512MC supports Quad SPI operation when using the “Quad Output Fast Read”, “Quad Output Fast Read with 4-byte address”, “Quad I/O Fast Read”, “Quad I/O Fast Read with 4-byte address” (6BH, 6CH, EBH and ECH) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD#/RESET# pins become IO2 and IO3. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set.

Hold

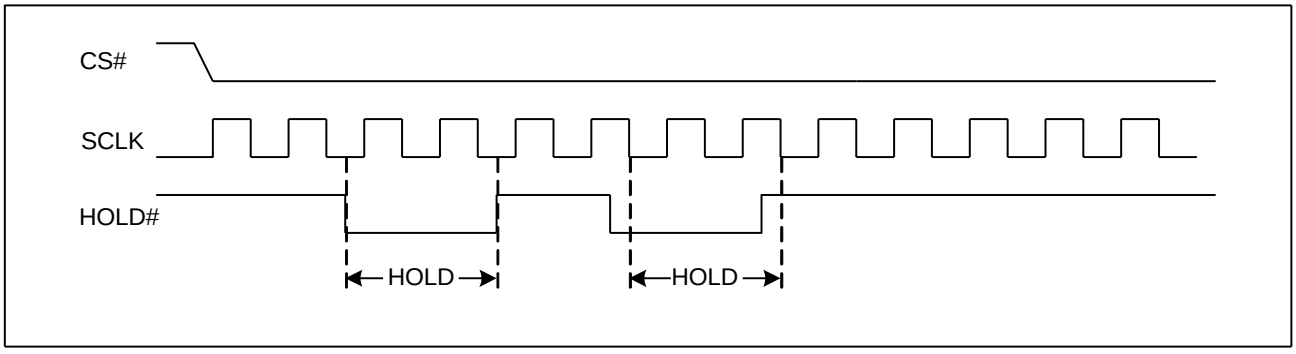
The HOLD/RST bit is used to determine whether HOLD# or RESET# function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=0, the pin7 acts as HOLD#, the HOLD# function is only available when QE=0, If QE=1, The HOLD# functions is disabled, the pin acts as dedicated data I/O pin.

The HOLD# signal goes low to stop any serial communications with the device, but doesn’t stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don’t care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

Figure 3 Hold Condition



RESET

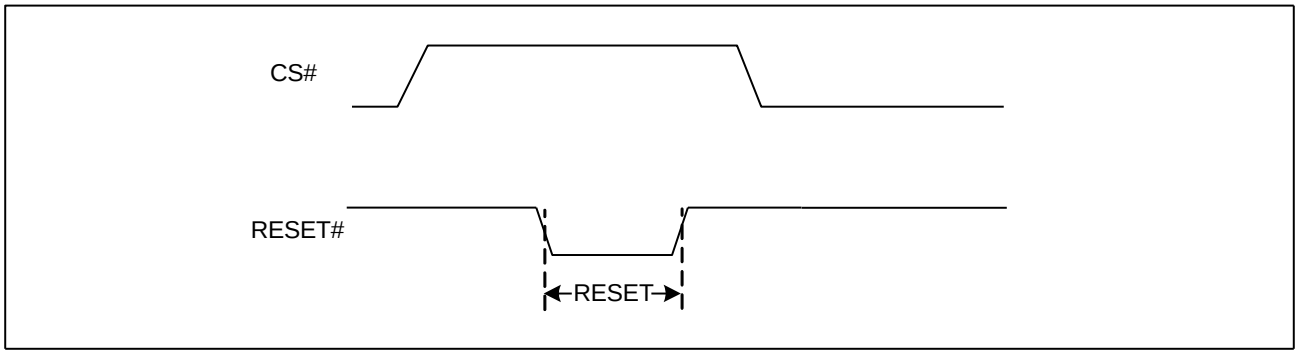
The RESET# pin allows the device to be reset by the control. For the WSON8 package, the pin7 can be configured as a RESET# pin depending on the status register setting, which need QE=0 and HOLD/RST=1. On the SOP16 package, a dedicated RESET# pin is provided and it is independent of QE bit setting.

The RESET# pin goes low for a period of tRLRH or longer will reset the flash. After reset cycle, the flash is at the following states:

-Standby mode

-All the volatile bits will return to the default status as power on.

Figure 4 RESET Condition



5. DATA PROTECTION

The GD25Q512MC provides the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  -Power-Up
  -Write Disable (WRDI)
  -Write Status Register (WRSR)
  -Page Program (PP)
  -Quad Page Program (QPP)
  -Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
- Software Protection Mode:
  -The Block Protect (BP3, BP2, BP1, and BP0) bits and Top Bottom (TB) bit define the section of the memory array that can be read but not change.
- Hardware Protection Mode: WP# going low to protected the BP0~BP3 bits, TB bit and SRP bit.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command.

5.1. Block Protection

Table 5. GD25Q512MC Protected area size (WPS=0)

Status Register Content					Memory Content			
TB	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	1023	03FF0000H-03FFFFFFH	64KB	Upper 1/1024
0	0	0	1	0	1022 to 1023	03FE0000H-03FFFFFFH	128KB	Upper 1/512
0	0	0	1	1	1020 to 1023	03FC0000H-03FFFFFFH	256KB	Upper 1/256
0	0	1	0	0	1016 to 1023	03F80000H-03FFFFFFH	512KB	Upper 1/128
0	0	1	0	1	1008 to 1023	03F00000H-03FFFFFFH	1MB	Upper 1/64
0	0	1	1	0	992 to 1023	03E00000H-03FFFFFFH	2MB	Upper 1/32
0	0	1	1	1	960 to 1023	03C00000H-03FFFFFFH	4MB	Upper 1/16
0	1	0	0	0	896 to 1023	03800000H-03FFFFFFH	8MB	Upper 1/8
0	1	0	0	1	768 to 1023	03000000H-03FFFFFFH	16MB	Upper 1/4
0	1	0	1	0	512 to 1023	02000000H-03FFFFFFH	32MB	Upper 1/2
1	0	0	0	1	0	00000000H-0000FFFFH	64KB	Lower 1/1024
1	0	0	1	0	0 to 1	00000000H-0001FFFFH	128KB	Lower 1/512
1	0	0	1	1	0 to 3	00000000H-0003FFFFH	256KB	Lower 1/256
1	0	1	0	0	0 to 7	00000000H-0007FFFFH	512KB	Lower 1/128
1	0	1	0	1	0 to 15	00000000H-000FFFFFH	1MB	Lower 1/64
1	0	1	1	0	0 to 31	00000000H-001FFFFFH	2MB	Lower 1/32
1	0	1	1	1	0 to 63	00000000H-003FFFFFH	4MB	Lower 1/16
1	1	0	0	0	0 to 127	00000000H-007FFFFFH	8MB	Lower 1/8
1	1	0	0	1	0 to 255	00000000H-00FFFFFFH	16MB	Lower 1/4
1	1	0	1	0	0 to 511	00000000H-01FFFFFFH	32MB	Lower 1/2

X	1	1	X	X	ALL	00000000H-03FFFFFFH	64MB	ALL
X	1	0	1	1	ALL	00000000H-03FFFFFFH	64MB	ALL

6. STATUS AND EXTENDED ADDRESS REGISTERS

6.1. Status Registers

Table 6 Status Register-1

No.	Bit Name	Description	Note
S0	WIP	Erase/Write In Progress	Volatile, read only
S1	WEL	Write Enable Latch	Volatile, read only
S2	BP0	Block Protect Bits	Non-volatile writable
S3	BP1	Block Protect Bits	Non-volatile writable
S4	BP2	Block Protect Bits	Non-volatile writable
S5	BP3	Block Protect Bits	Non-volatile writable
S6	QE	Quad Enable	Non-volatile writable
S7	SRP	Status Register Protection	Non-volatile writable

Table 7 Status Register-2

No.	Bit Name	Description	Note
S8	DRV0	Output Driver Strength	Non-volatile writable
S9	DRV1	Output Driver Strength	Non-volatile writable
S10	HOLD/RST	HOLD# or Reset# Function	Non-volatile writable
S11	TB	Top/Bottom Protect Bit	Non-volatile writable
S12	ADP	Power Up Address Mode	Non-volatile writable
S13	ADS	Current Address Mode	Volatile, read only
S14	LC0	Latency Code 0	Non-volatile writable
S15	LC1	Latency Code 1	Non-volatile writable

Table 8 Status Register-3

No.	Bit Name	Description	Note
S16	LB1	OTP lock bits	Non-volatile writable (OTP)
S17	LB2	OTP lock bits	Non-volatile writable (OTP)
S18	SUS_P	Program Suspend	Volatile, read only
S19	SUS_E	Erase Suspend	Volatile, read only
S20	LB3	OTP lock bits	Non-volatile writable (OTP)
S21	PE	Program Error bit	Volatile, read only
S22	EE	Erase Error bit	Volatile, read only
S23	WPS	Write Protect Selection	Non-volatile writable

The status and control bits of the Status Register are as follows:

WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or

Erase command is accepted.

TB bit

The Top Bottom (TB) bit is non-volatile (OTP). The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, and BP0), starting from Top or Bottom of the memory array. The TB bit is defaulted as “0”, which means Top area protect. When it is set to “1”, the protect area will change to Bottom area of the memory device. This bit is written with the Write Status Register (WRSR) command.

BP3, BP2, BP1, BP0 bits

The Block Protect (BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed only if none sector or block is protected.

SRP bit

The Status Register Protect (SRP) bit is non-volatile Read/Write bits in the status register. The SRP bit controls the method of write protection: software protection and hardware protection.

Table 9 Status Register Protect (SRP) bit

SRP	#WP	Status Register	Description
0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
1	0	Hardware Protected	WP#=0, the Status Register locked and can not be written to.
1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.

QE bit

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# / RESET# pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the WP# or HOLD# / RESET# pins are tied directly to the power supply or ground)

LB3, LB2, LB1, bits.

The LB3, LB2, LB1, bits are non-volatile One Time Program (OTP) bits in Status Register (S16, S17, S20) that provide the write protect control and status to the Security Registers. The default state of LB3-LB1 are 0, the security registers are unlocked. The LB3-LB1 bits can be set to 1 individually using the Write Register instruction. The LB3-LB1 bits are One Time Programmable, once its set to 1, the Security Registers will become read-only permanently.

SUS_E, SUS_P bit

The SUS_E and SUS_P bit are read only bit in the status register (S18 and S19) that are set to 1 after executing an Program/Erase Suspend (75H) command (The Erase Suspend will set the SUS_E to 1,and the Program Suspend will set the SUS_P to 1). The SUS_E and SUS_P bit are cleared to 0 by Program/Erase Resume (7AH) command as well as a power-down, power-up cycle.

WPS

The WPS Bit is used to select which Write Protect scheme should be used. When WPS=0, the device will use the combination of TB, BP (3:0) bits to protect a specific area of the memory array. When WPS=1, the device will utilize the Advanced Block Protection to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1

upon device power on or after reset.

DRV1/DRV0

The DRV1&DRV0 bits are used to determine the output driver strength for the Read operations.

Table 10 Driver Strength for Read Operations

DRV1,DRV0	Driver Strength
00	100%
01	75%
10	50% (Default)
11	25%

HOLD/RST

The HOLD/RST bit is used to determine whether HOLD# or RESET# function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=0, the pin acts as HOLD#, When the HOLD/RST=1, the pin acts as RESET#. However, the HOLD# or RESET# function are only available when QE=0, If QE=1, The HOLD# and RESET# functions are disabled, the pin acts as dedicated data I/O pin.

PE

The Program Error (PE) bit is a read only bit that indicates a program failure. It will also be set when the user attempts to program a protected array sector or access the locked OTP space.

Error bits must be reset by CLEAR FLAG STATUS REGISTER command (30H).

EE

The Erase Error (EE) bit is a read only bit that indicates an erase failure. It will also be set when the user attempts to erase a protected array sector or access the locked OTP space.

Error bits must be reset by CLEAR FLAG STATUS REGISTER command (30H).

LC1, LC0 bits

The Latency Code (LC) selects the mode and number of dummy cycles between the end of address and the start of read data output for all read commands.

Some read commands send mode bits following the address to indicate that the next command will be of the same type with an implied, rather than an explicit, instruction. The next command thus does not provide an instruction byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands.

Dummy cycles provide additional latency that is needed to complete the initial read access of the flash array before data can be returned to the host system. Some read commands require additional latency cycles as the SCLK frequency is increased.

The following latency code tables provide different latency settings that are configured by GigaDevice.

Table 11 Latency Code and Frequency Table

LC	Freq. (MHz)	Read (03h, 13h)		Freq. (MHz)	Fast Read (0Bh, 0Ch)		Freq. (MHz)	Read Dual Out (3Bh, 3Ch)		Read Quad Out (6Bh, 6Ch)		Dual I/O Read (BBh, BCh)		Quad I/O Read (EBh, ECh)	
		Mode	Dummy		Mode	Dummy		Mode	Dummy	Mode	Dummy	Mode	Dummy	Mode	Dummy
11	≤50	0	0	≤50	0	0	≤80	0	6	0	6	4	0	2	4
00	≤80	0	0	≤104	0	8	≤80	0	8	0	8	4	0	2	4
01 or 10	≤104	-	-	≤104	0	8	≤104	0	8	0	8	4	2	2	6

Note:

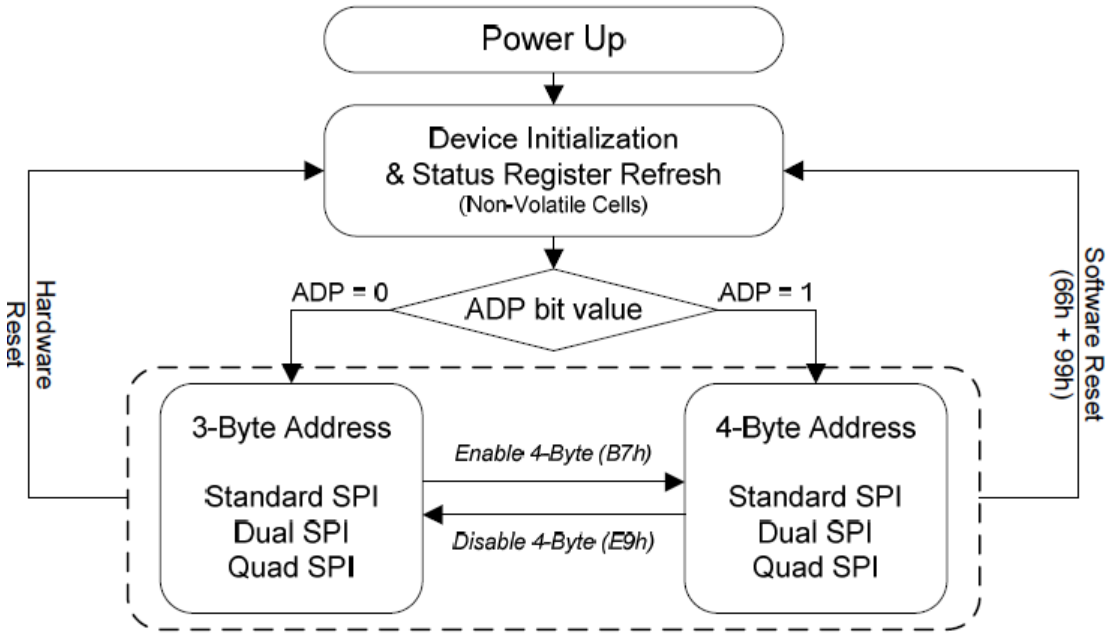
1. The default value of latency code is 00.
2. Not 100% tested in production.

ADS

The Address Status (ADS) bit is a read only bit that indicates the current address mode the device is operating in. The device is in 3-byte address mode when ADS=0 (default), and in 4-byte address mode when ADS=1.

ADP

The Address Power-up (ADP) bit is a non-volatile writable bit that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period. When ADP=0(factory default), the device will power up into 3-byte address mode, the Extended Address Register must be used to access memory regions beyond 128Mb. When ADP=1, the device will power up into 4-byte address mode directly.



6.2. Extended Address Register

Table 12 Extended Address Register

EA7	EA6	EA5	EA4	EA3	EA2	EA1	EA0
A31	A30	A29	A28	A27	A26	A25	A24

The extended address register is only used when the address mode is 3-byte mode, as to set the higher address.

When the device is 512Mb, A25 is the highest address bit. When the device is 256Mb, A24 is the highest address bit. A31~A26 are reserved for higher density from 1Gb ~ 32Gb.

7. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

Every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

When the device is in 3-byte address mode (ADS=0), please refer to command set in table13 & table14. When the device is in 4-byte address mode (ADS=1), please refer to command set in table13 & table15.

Extended Address Register setting is effective to achieve A31-A24, accompanying A23-A0 within the instruction, when commands listed in table14 are executed.

Extended Address Register setting is ignored when A31-A24 are given in the instruction listed in table 3 and some specific instruction from table13 (13H, 0CH, 3CH, 6CH, BCH, ECH).

Table 13. Commands (Standard/Dual/Quad SPI, 3-byte & 4-byte address mode)

Command Name	Add Mode	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Write Enable	3 & 4	06H						
Write Disable	3 & 4	04H						
Read Status Register-1	3 & 4	05H	(S7-S0)					(cont.)
Read Status Register-2	3 & 4	35H	(S15-S8)					(cont.)
Read Status Register-3	3 & 4	15H	(S23-S16)					
Write Status Register-1	3 & 4	01H	(S7-S0)					
Write Status Register-2	3 & 4	31H	(S15-S8)					
Write Status Register-3	3 & 4	11H	(S23-S16)					
Read Extended Addr. Register	3 & 4	C8H	(EA7-EA0)					
Write Extended Addr. Register	3 & 4	C5H	(EA7-EA0)					
Chip Erase	3 & 4	C7/60H						
Enable Reset	3 & 4	66H						
Reset	3 & 4	99H						
Program/Erase Suspend	3 & 4	75H						

Program/Erase Resume	3 & 4	7AH						
Set Burst with Wrap (5)	3 & 4	77H	dummy W7-W0					
Release From Deep Power-Down	3 & 4	ABH						
Read Device ID	3 & 4	ABH	dummy	dummy	dummy	(DID7-DID0)		(cont.)
Deep Power-Down	3 & 4	B9H						
Manufacturer/ Device ID	3 & 4	90H	dummy	dummy	00H	(MID7-MID0)	(DID7-DID0)	(cont.)
Read Identification	3 & 4	9FH	(MID7-MID0)	(JDID15-JDID8)	(JDID7-JDID0)			(cont.)
Enter 4-Byte Address Mode	3 & 4	B7H						
Exit 4-Byte Address Mode	3 & 4	E9H						
Read Data with 4-Byte Address	3 & 4	13H	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read with 4-Byte Address	3 & 4	0CH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Fast Read Dual Output with 4-Byte Address (1)	3 & 4	3CH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Fast Read Quad Output with 4-Byte Address (3)	3 & 4	6CH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Fast Read Dual I/O with 4-Byte Address (2)	3 & 4	BCH	A31-A24 A23-A 16	A15-A8 A7-A0	M7-M0 (D7-D0)			
Fast Read Quad I/O with 4-Byte Address (4)	3 & 4	ECH	A31-A24 A23-A 16 A15-A8 A7-A0	M7-M0 dummy dummy (D7-D0)				
Page Program with 4-Byte Address	3 & 4	12H	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	Next byte
Quad Page Program with 4-Byte Address	3 & 4	3EH	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)(3)	
Sector Erase with 4-Byte Address	3 & 4	21H	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase(32K) with 4-Byte Address	3 & 4	5CH	A31-A24	A23-A16	A15-A8	A7-A0		
Block	3 & 4	DCH	A31-A24	A23-A16	A15-A8	A7-A0		

Erase(64K) with 4-Byte Address								
Clear SR Flags	3 & 4	30H						

Table 14 Commands (Standard/Dual/Quad SPI, 3-byte address)

Command Name	Add Mode	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Read Data	3	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(cont.)
Fast Read	3	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)
Dual Output Fast Read (1)	3	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)	(cont.)
Dual I/O Fast Read (2)	3	BBH	A23-A8(2)	A7-A0 M7-M0(2)	(D7-D0)(1)			(cont.)
Quad Output Fast Read (3)	3	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(3)	(cont.)
Quad I/O Fast Read (4)	3	EBH	A23-A0 M7-M0(4)	dummy	(D7-D0)(3)			(cont.)
Page Program	3	02H	A23-A16	A15-A8	A7-A0	(D7-D0)	Next byte	
Quad Page Program	3	32H	A23-A16	A15-A8	A7-A0	(D7-D0)(3)		
Sector Erase	3	20H	A23-A16	A15-A8	A7-A0			
Block Erase(32K)	3	52H	A23-A16	A15-A8	A7-A0			
Block Erase(64K)	3	D8H	A23-A16	A15-A8	A7-A0			
Read Serial Flash Discoverable Parameter	3	5AH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)
Read Unique ID	3	4BH	dummy	dummy	dummy	dummy	(UID63-UID0)	
Erase Security Registers (6)	3	44H	A23-A16	A15-A8	A7-A0			
Program Security Registers (6)	3	42H	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)	
Read Security Registers (6)	3	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	

Table 15. Commands (Standard/Dual/Quad SPI, 4-byte address)

Command Name	Add Mode	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Bytes-7	n-Bytes
Read Data	4	03H	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)		(cont.)
Fast Read	4	0BH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)
Dual Output Fast Read (1)	4	3BH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)	(cont.)
Dual I/O Fast Read (2)	4	BBH	A31-A24 A23-A16	A15-A8 A7-A0	M7-M0(2) dummy	(D7-D0)(1)			
Quad Output Fast Read (3)	4	6BH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)	(cont.)
Quad I/O Fast Read (4)	4	EBH	A31-A24 A23-A16 A15-A8 A7-A0	M7-M0(4) dummy dummy (D7-D0)(3)					(cont.)
Page Program	4	02H	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)	(cont.)
Quad Page Program	4	32H	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)(3)		(cont.)
Sector Erase	4	20H	A31-A24	A23-A16	A15-A8	A7-A0			

Block Erase(32K)	4	52H	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase(64K)	4	D8H	A31-A24	A23-A16	A15-A8	A7-A0			
Read Serial Flash Discoverable Parameter	4	5AH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)
Read Unique ID	4	4BH	dummy	dummy	dummy	dummy	dummy	(UID63-UID0)	
Erase Security Registers (6)	4	44H	A31-A24	A23-A16	A15-A8	A7-A0			
Program Security Registers (6)	4	42H	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)	(cont.)
Read Security Registers (6)	4	48H	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)

NOTE:

1. Dual Output data

   IO0 = (D6, D4, D2, D0)

   IO1 = (D7, D5, D3, D1)

2. Dual Input Address

   IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0

   IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data

   IO0 = (D4, D0, …..)

   IO1 = (D5, D1, …..)

   IO2 = (D6, D2, …..)

   IO3 = (D7, D3,…..)

4. Quad Input Address

   IO0 = A20, A16, A12, A8, A4, A0, M4, M0

   IO1 = A21, A17, A13, A9, A5, A1, M5, M1

   IO2 = A22, A18, A14, A10, A6, A2, M6, M2

   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

5. Dummy bits and Wrap Bits

   IO0 = (x, x, x, x, x, x, W4, x)

   IO1 = (x, x, x, x, x, x, W5, x)

   IO2 = (x, x, x, x, x, x, W6, x)

   IO3 = (x, x, x, x, x, x, W7, x)

6. Security Registers Address

   Security Register1: A23-A16=00H, A15-A8=10H, A7-A0= Byte Address;

   Security Register2: A23-A16=00H, A15-A8=20H, A7-A0= Byte Address;

   Security Register3: A23-A16=00H, A15-A8=30H, A7-A0= Byte Address.

Table of ID Definitions:

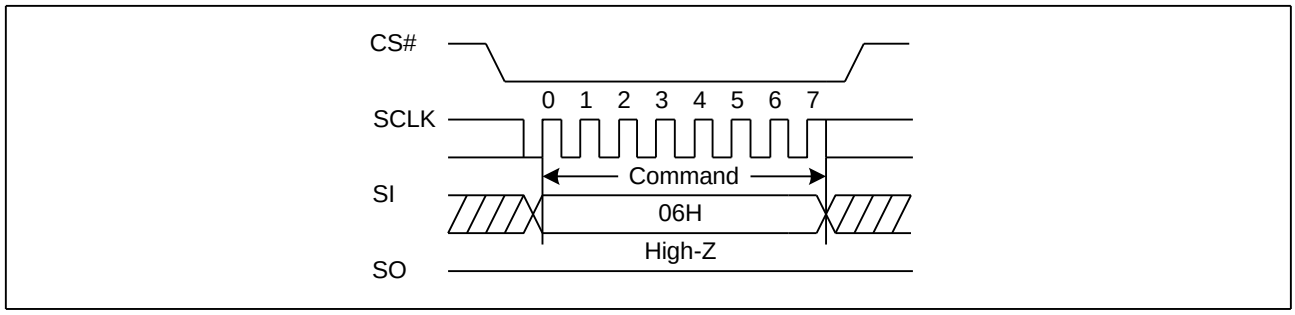
GD25Q512MC

Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9FH	C8	40	20
90H	C8		19
ABH			19

7.1. Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Quad Page Program (QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR). The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

Figure 5 Write Enable Sequence Diagram



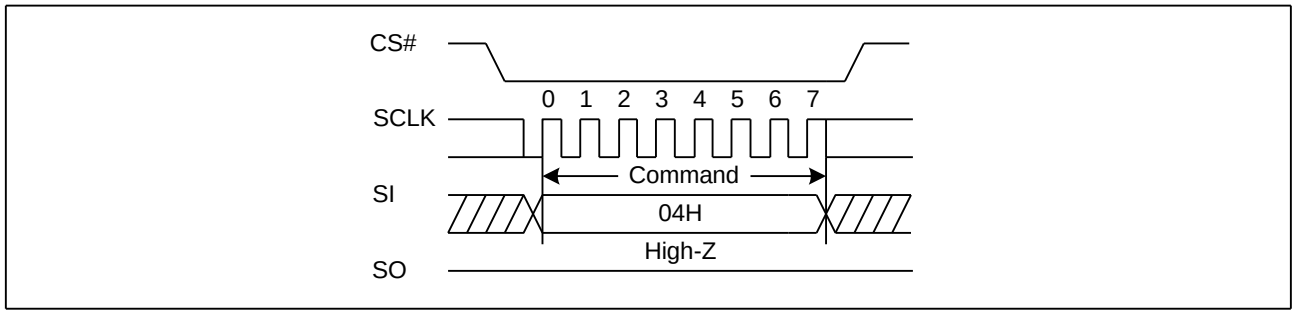
7.2. Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit may be set to a 0 by issuing the Write Disable (WRDI) command to disable Page Program (PP), Quad Page Program (QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), that require WEL be set to 1 for execution. The WRDI command can be used by the user to protect memory areas against inadvertent writes that can possibly corrupt the contents of the memory. The WRDI command is ignored during an embedded operation while WIP bit =1.

The WEL bit is reset by following condition: Write Disable command (WRDI), Power-up, and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

The Write Disable command sequence: CS# goes low →Sending the Write Disable command →CS# goes high.

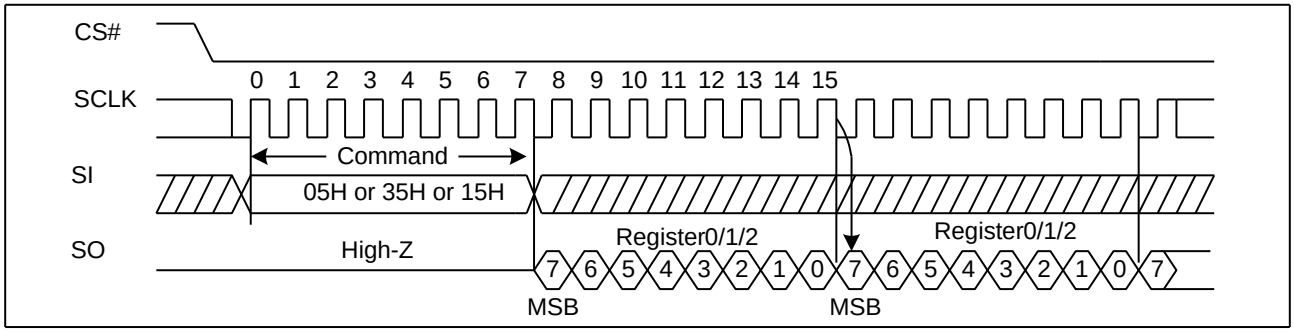
Figure 6 Write Disable Sequence Diagram



7.3. Read Status Register (RDSR) (05H or 35H or 15H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H” / “35H” / “15H”, the SO will output Status Register bits S7~S0 / S15-S8 / S16-S23.

Figure 7 Read Status Register Sequence Diagram



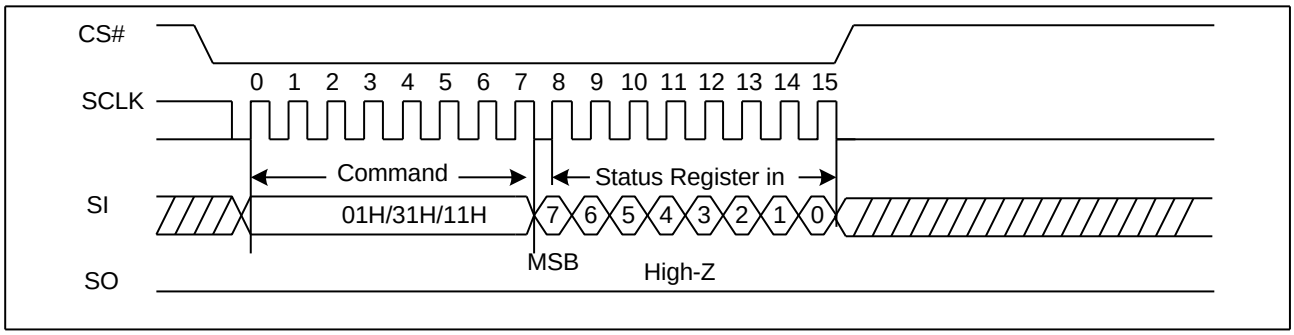
7.4. Write Status Register (WRSR) (01H or 31H or 11H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S22, S21, S19, S18, S13, S1 and S0 of the Status Register. CS# must be driven high after the eighth of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP) bits in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bits and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

Figure 8 Write Status Register Sequence Diagram



7.5. Read Data Bytes (READ 03H or 4READ 13H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_R, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 9 Read Data Bytes Sequence Diagram (ADS=0)

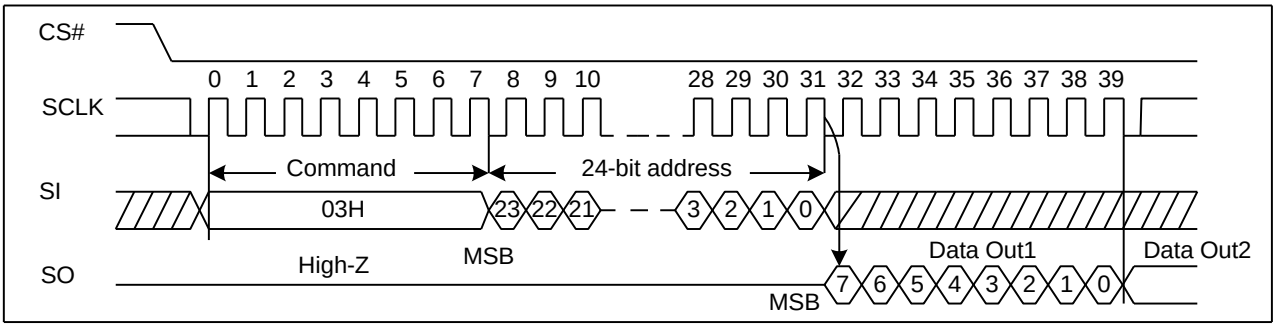


Figure 10 Read Data Bytes Sequence Diagram (ADS=1)

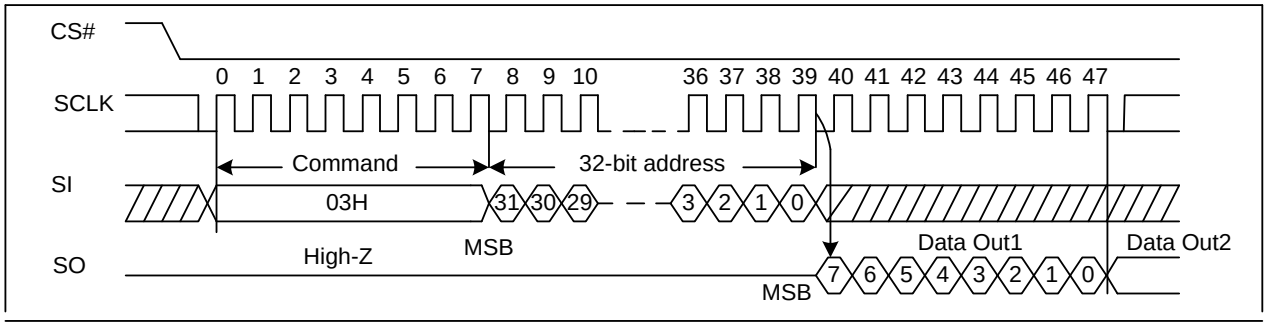
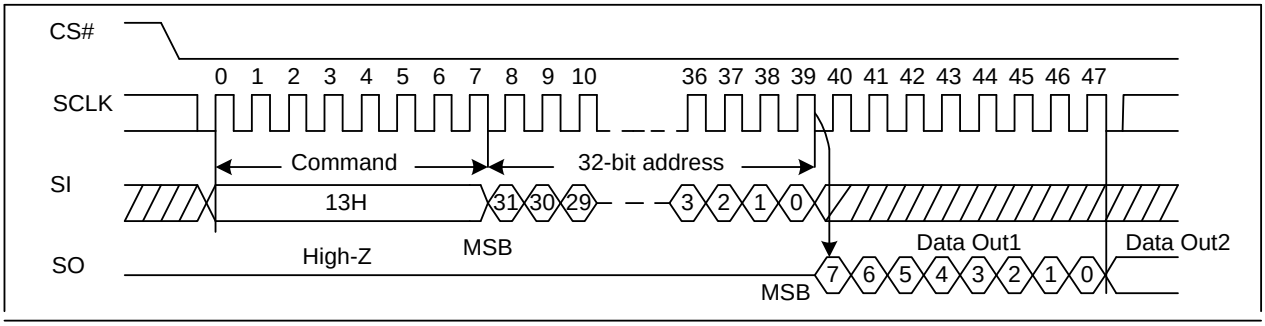


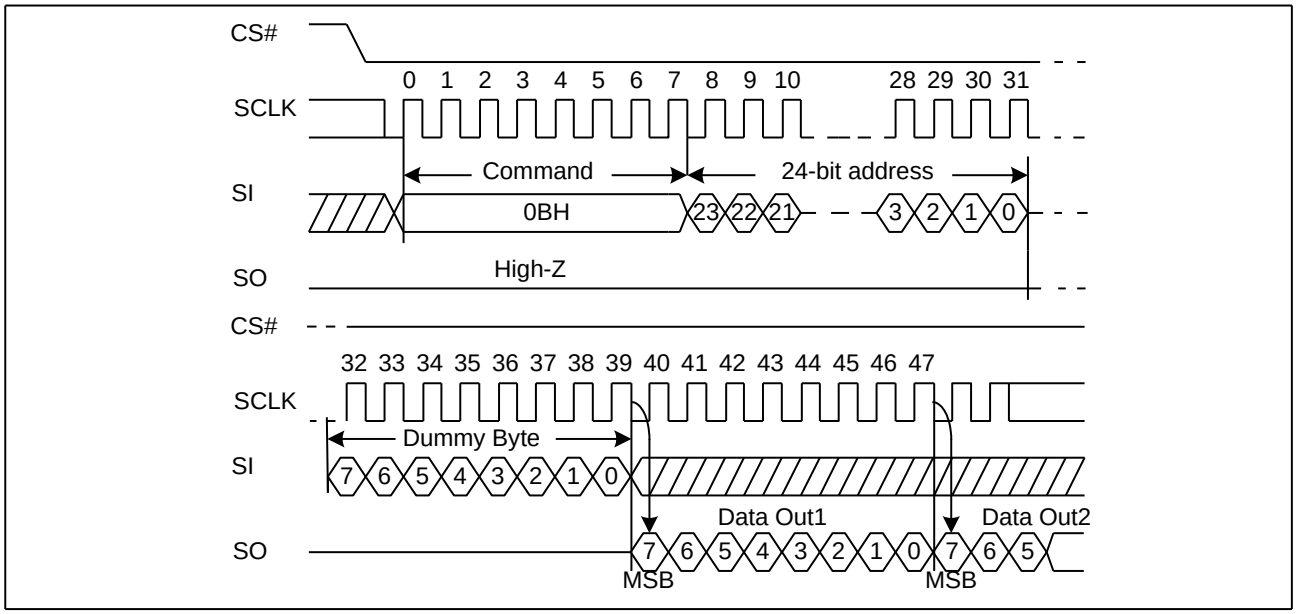
Figure 11 Read Data with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)



7.6. Read Data Bytes at Higher Speed (Fast Read 0BH or 4Fast Read 0CH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_C, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

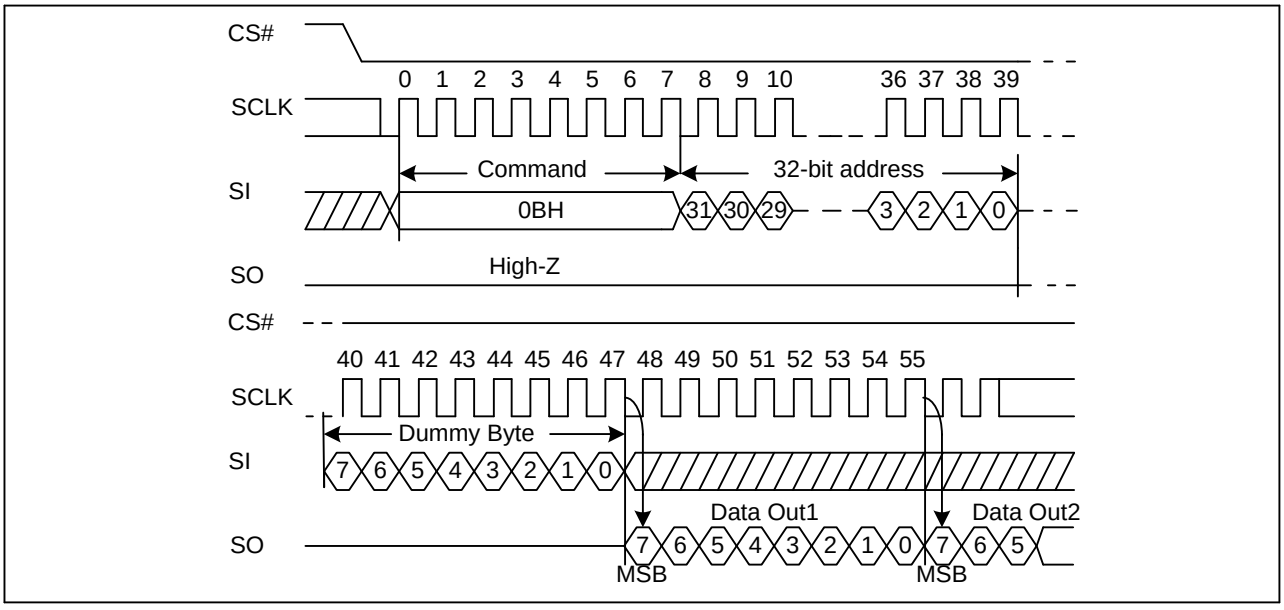
Figure 12 Read Data Bytes at Higher Speed Sequence Diagram (ADS=0)



Note:

1. The dummy clock number is configurable.

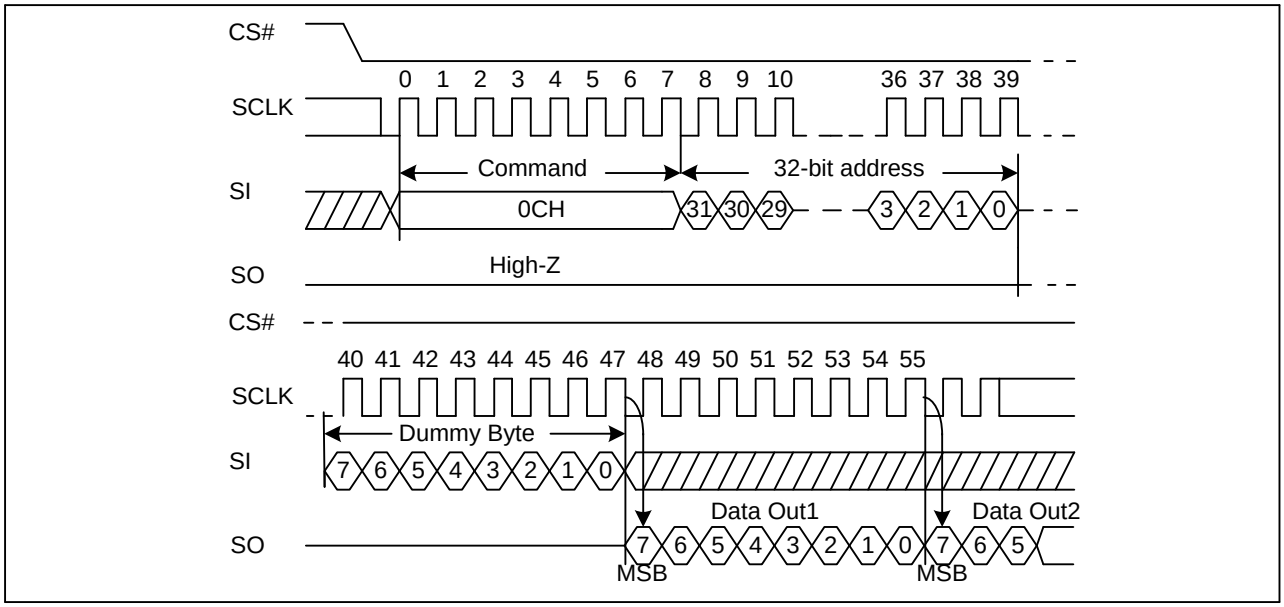
Figure 13 Read Data Bytes at Higher Speed Sequence Diagram (ADS=1)



Note:

1. The dummy clock number is configurable.

Figure 14 Fast Read with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)



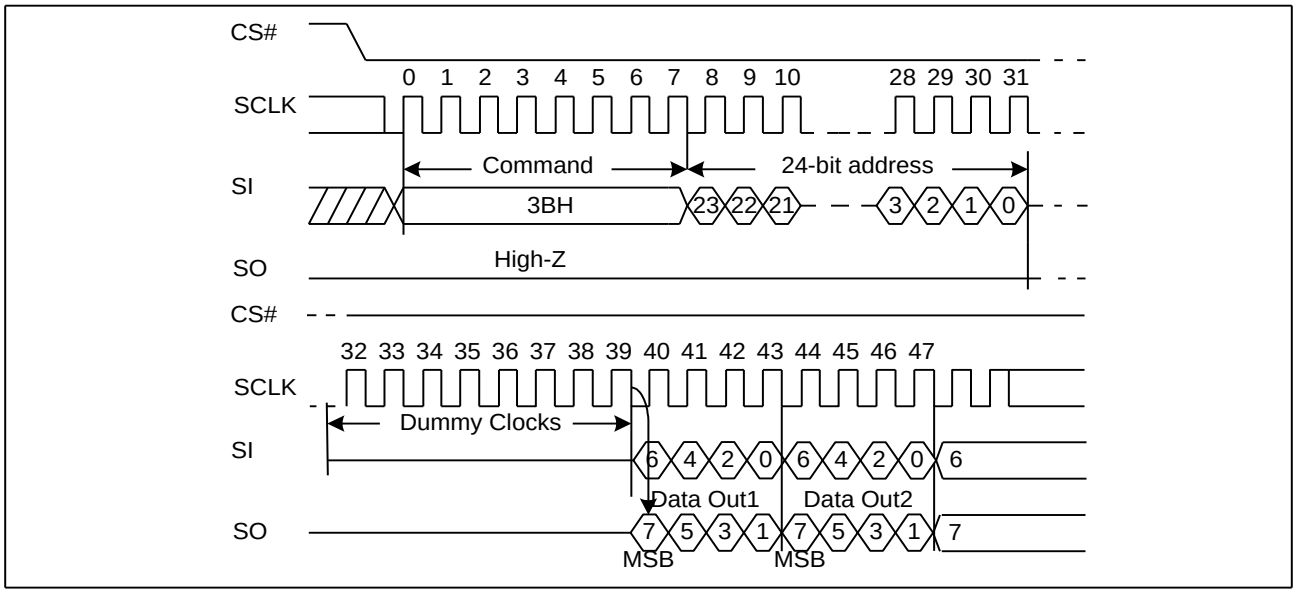
Note:

1. The dummy clock number is configurable.

7.7. Dual Output Fast Read (DOFR 3BH or 4DOFR 3CH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure 16. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

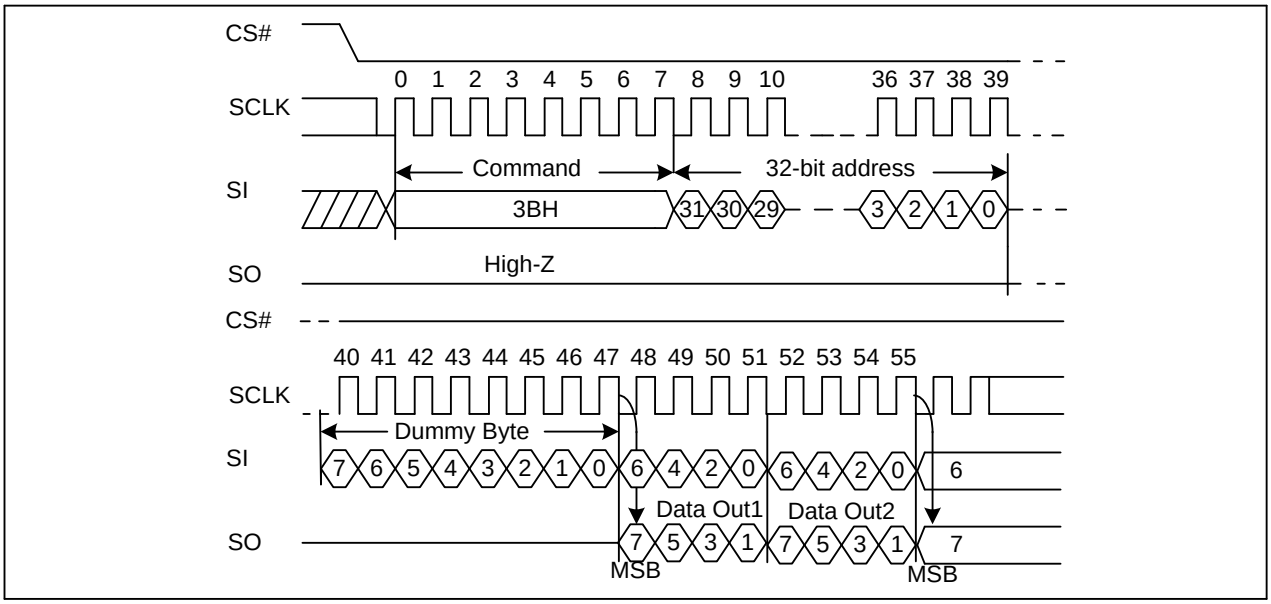
Figure 15 Dual Output Fast Read Sequence Diagram (ADS=0)



Note:

1. The dummy clock number is configurable.

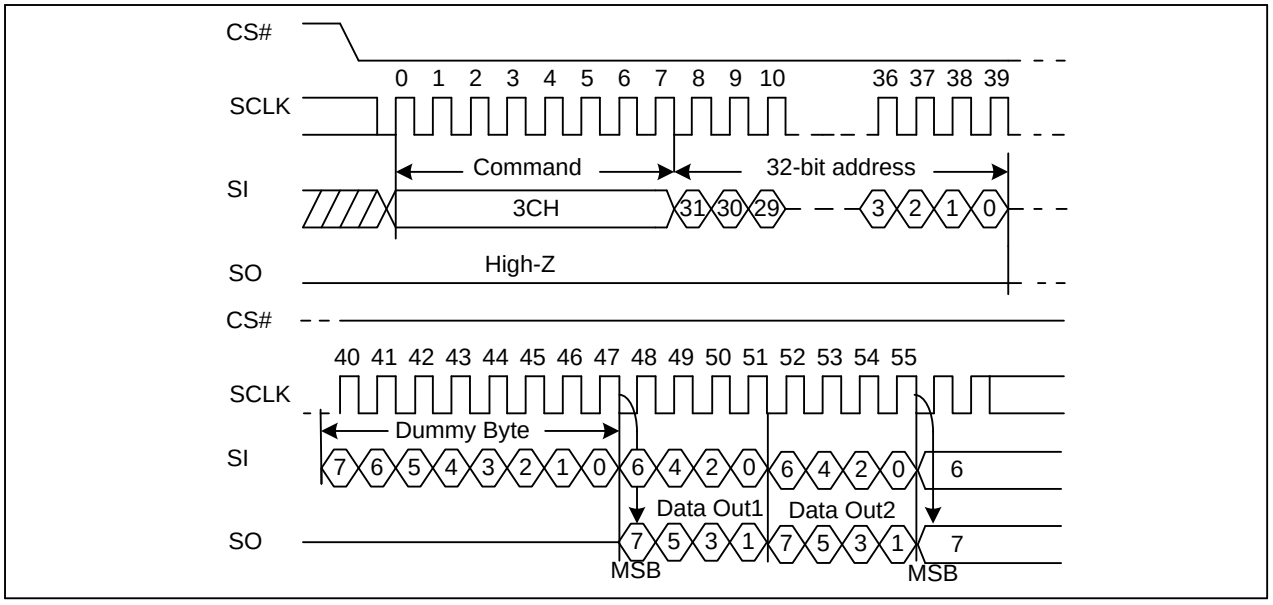
Figure 16 Dual Output Fast Read Sequence Diagram (ADS=1)



Note:

1. The dummy clock number is configurable.

Figure 17 Dual Output Fast Read with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)



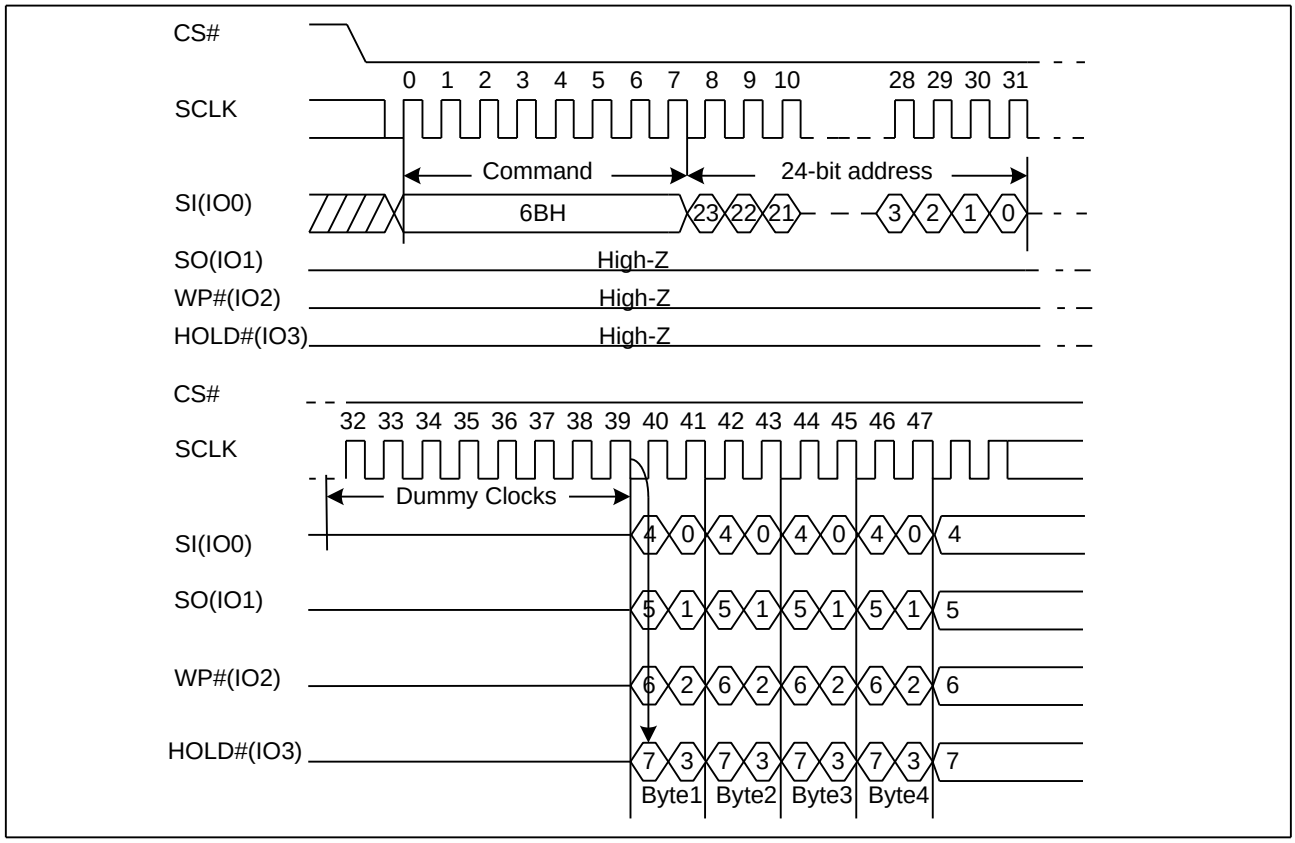
Note:

1. The dummy clock number is configurable.

7.8. Quad Output Fast Read (QOFR 6BH or 4QOFR 6CH)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in followed Figure19. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

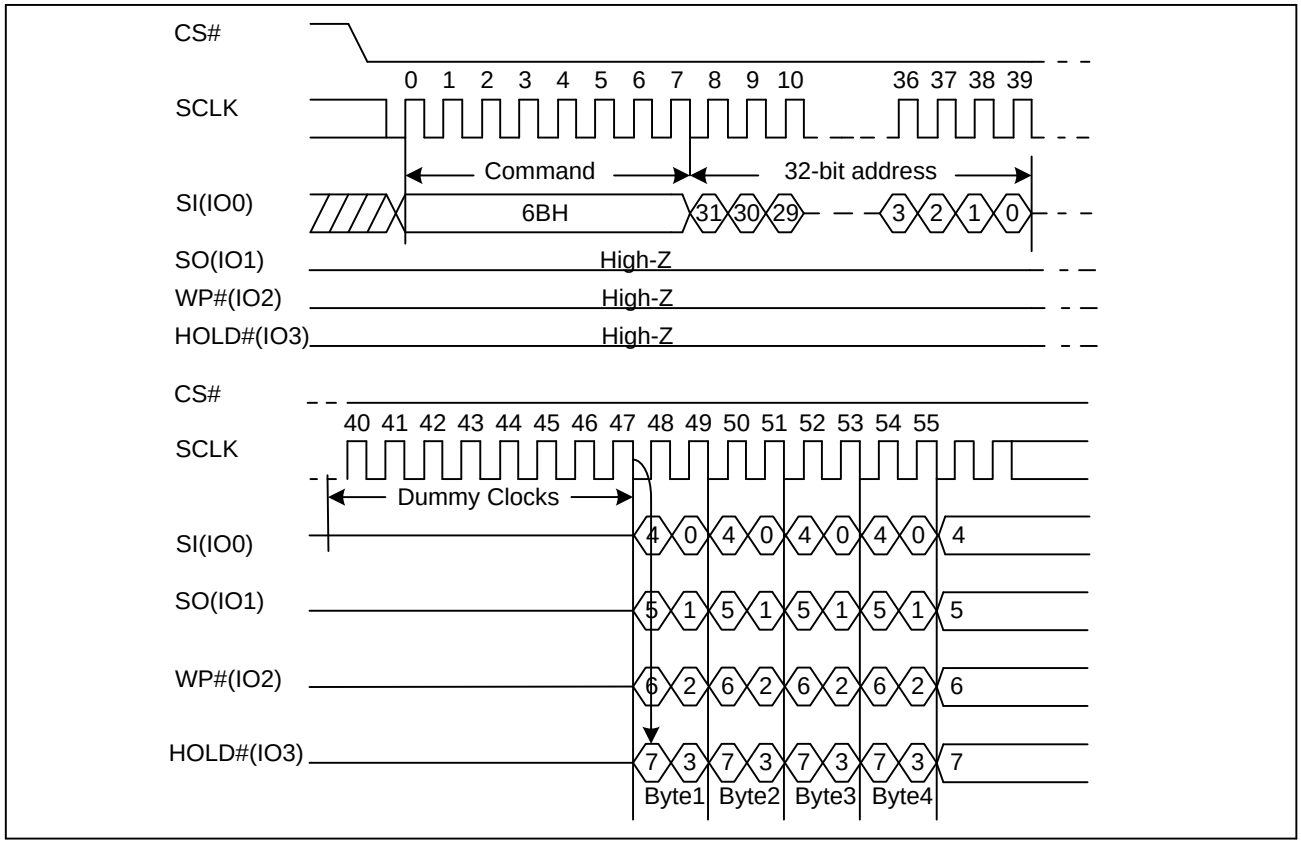
Figure 18 Quad Output Fast Read Sequence Diagram (ADS=0)



Note:

1. The dummy clock number is configurable.

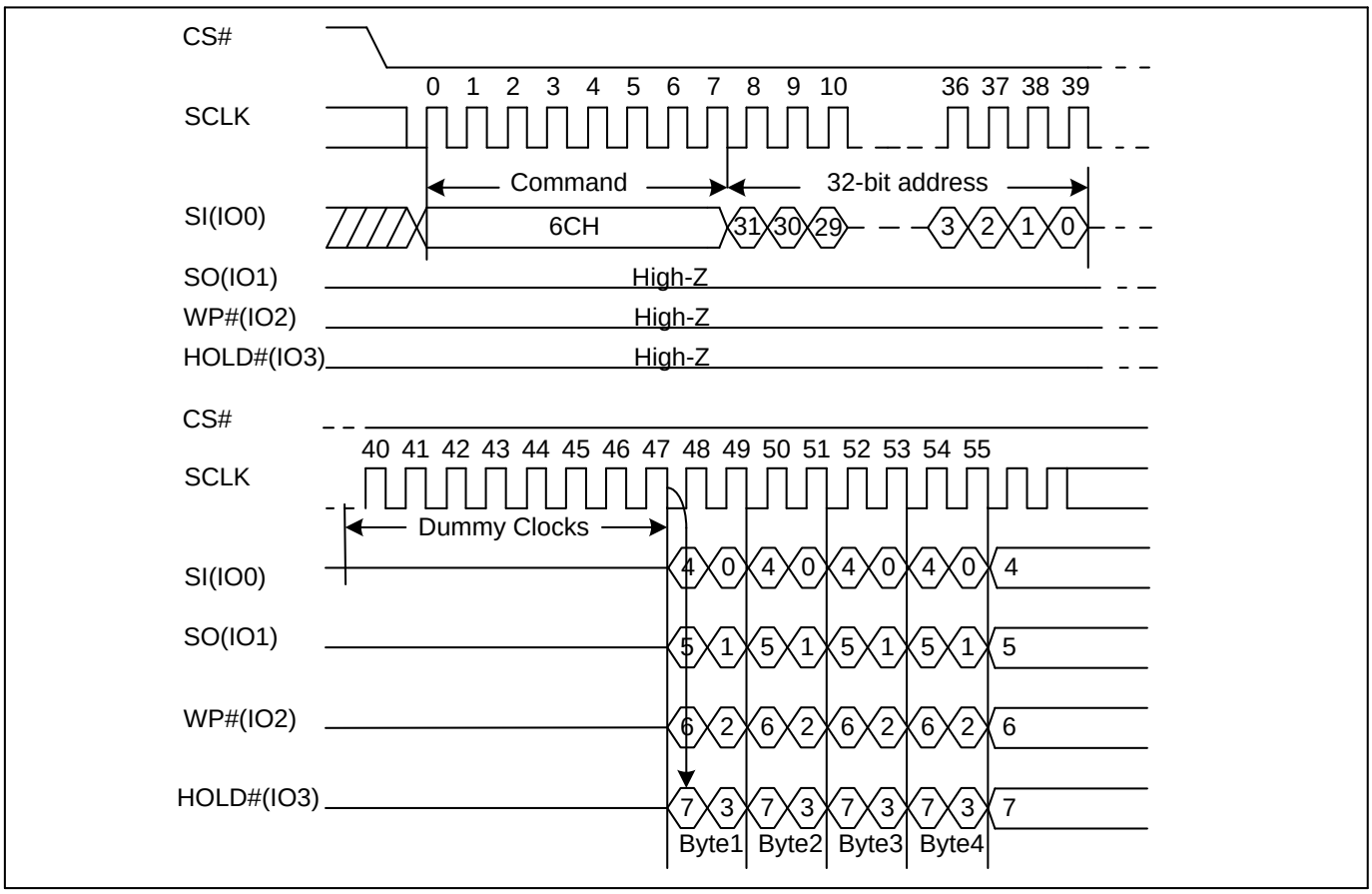
Figure 19 Quad Output Fast Read Sequence Diagram (ADS=1)



Note:

1. The dummy clock number is configurable.

Figure 20 Fast Read Quad Output with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)



Note:

1. The dummy clock number is configurable.

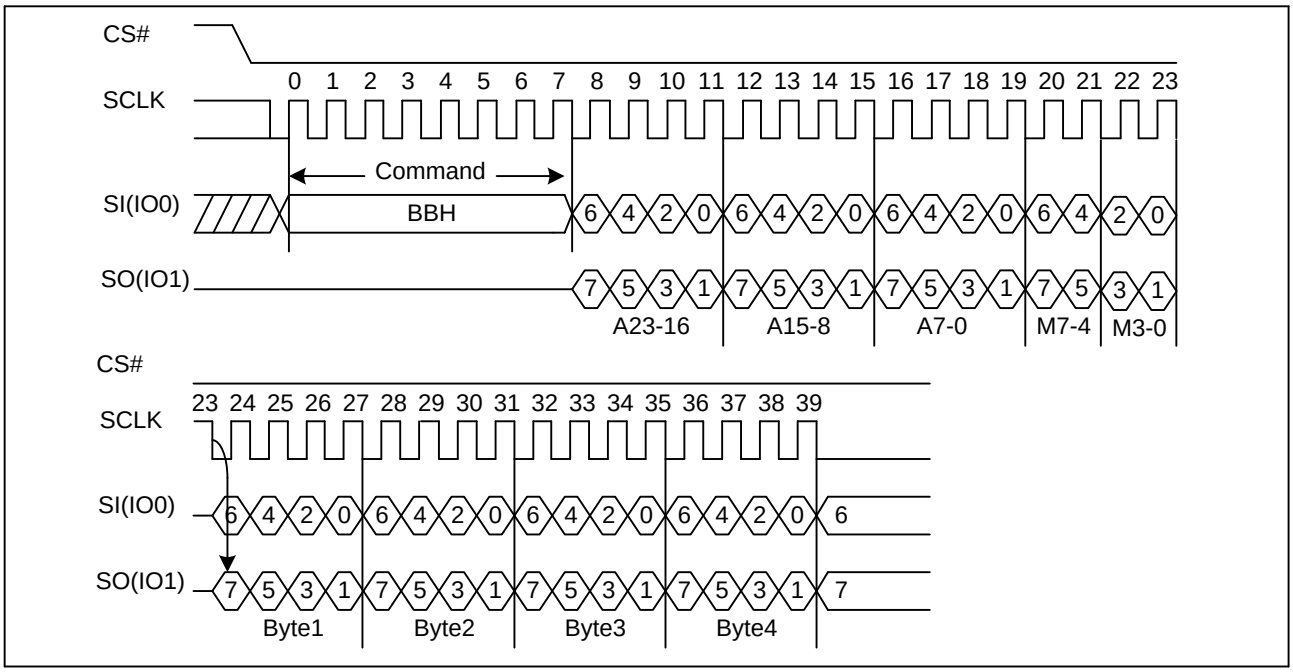
7.9. Dual I/O Fast Read (DIOFR BBH or 4DIOFR BCH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure22. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Dual I/O Fast Read with “Continuous Read Mode”

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-4) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in followed Figure23. If the “Continuous Read Mode” bits (M5-4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A Reset command can be used to reset (M5-4) before issuing normal command.

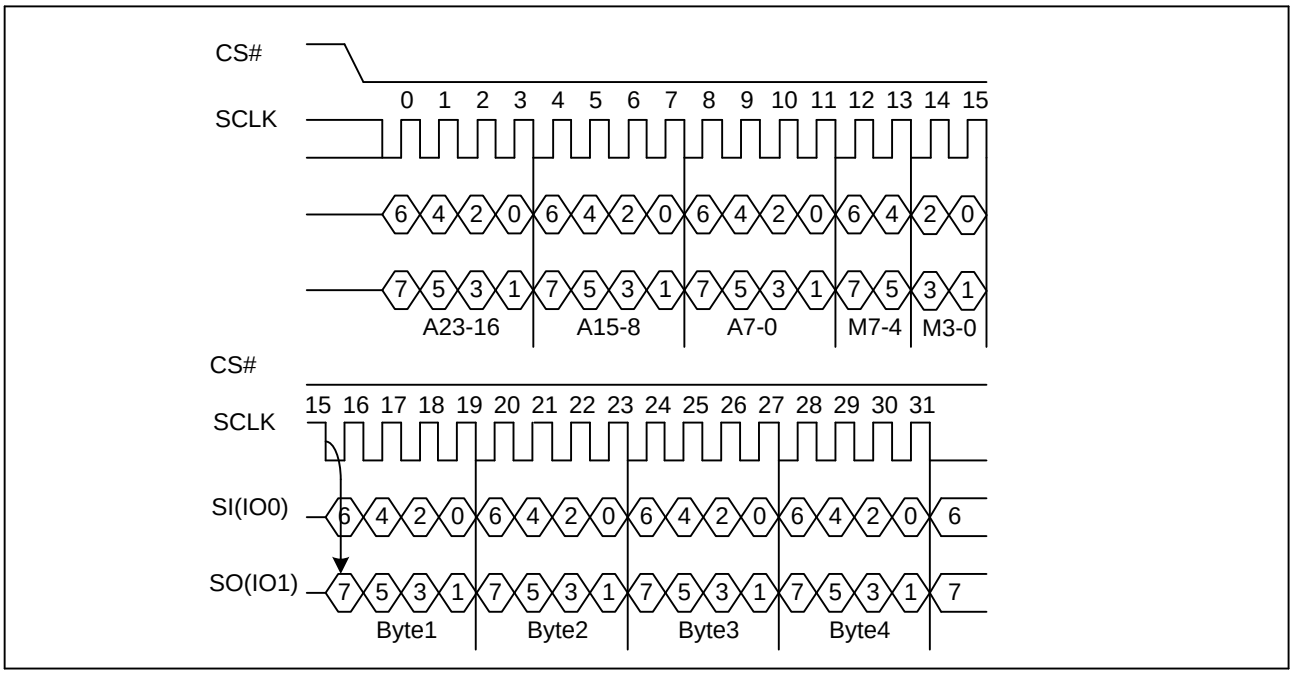
Figure 21 Dual I/O Fast Read Sequence Diagram (M5-4≠ (1, 0), ADS=0)



Note:

1. The dummy clock number is configurable.

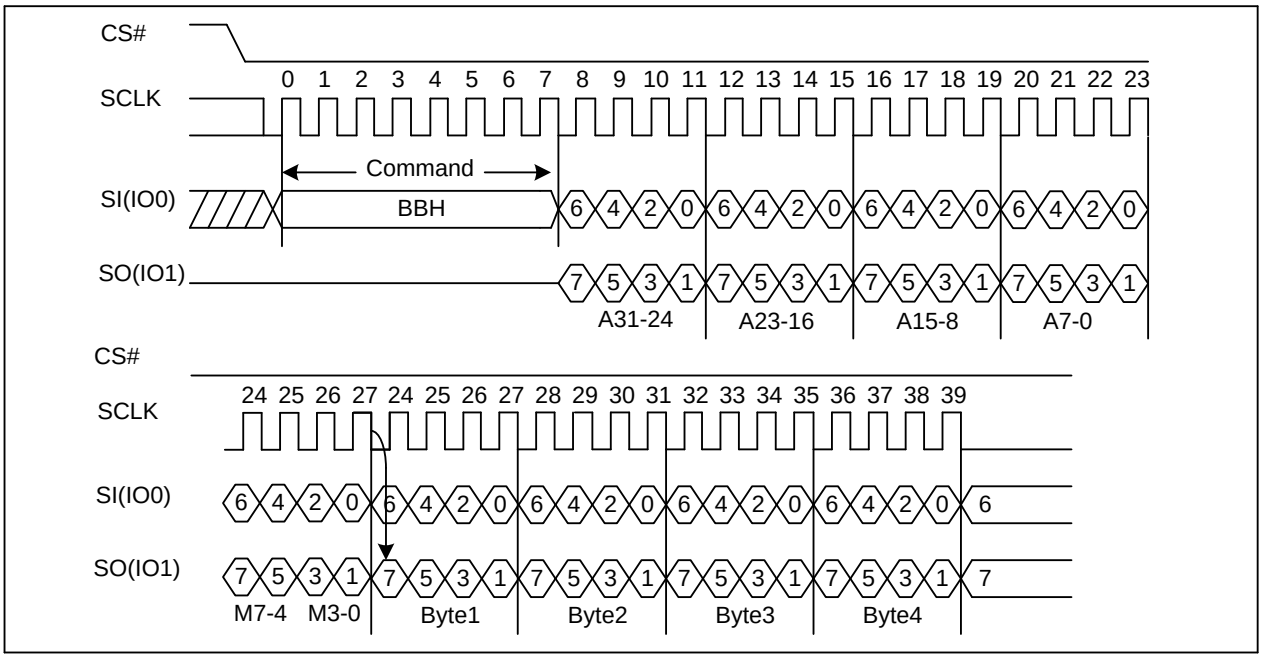
Figure 22 Dual I/O Fast Read Sequence Diagram (M5-4= (1, 0), ADS=0)



Note:

1. The dummy clock number is configurable.

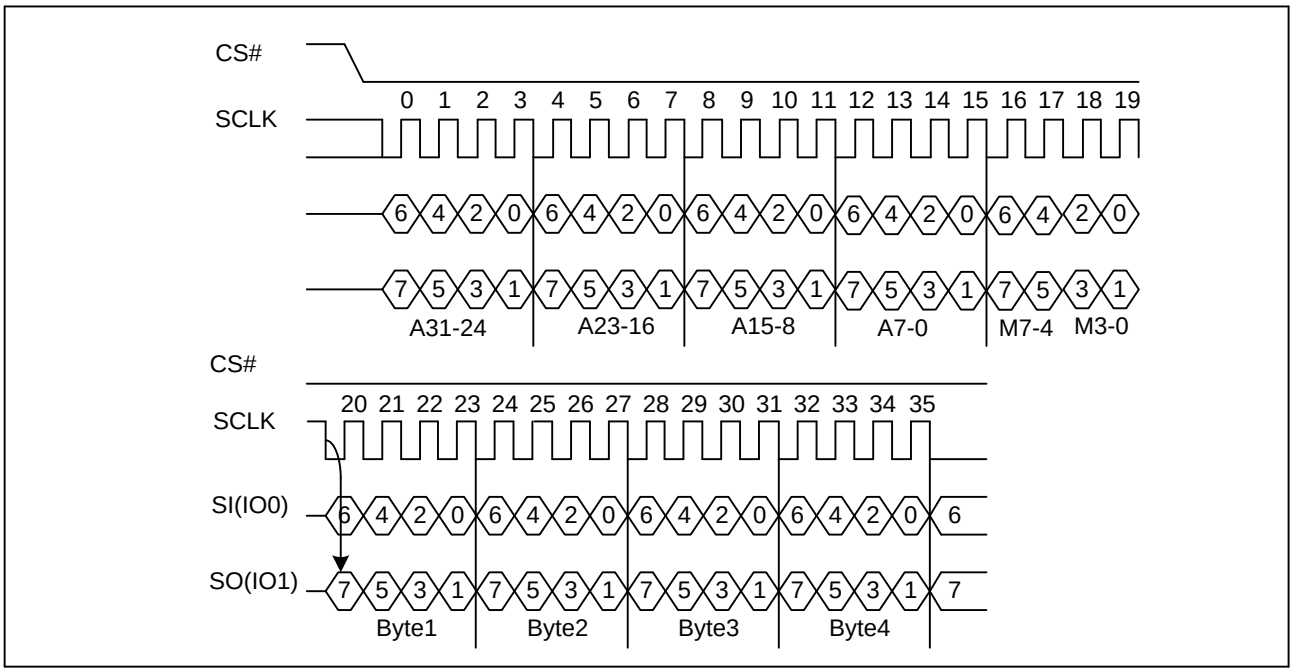
Figure 23 Dual I/O Fast Read Sequence Diagram (M5-4≠ (1, 0), ADS=1)



Note:

1. The dummy clock number is configurable.

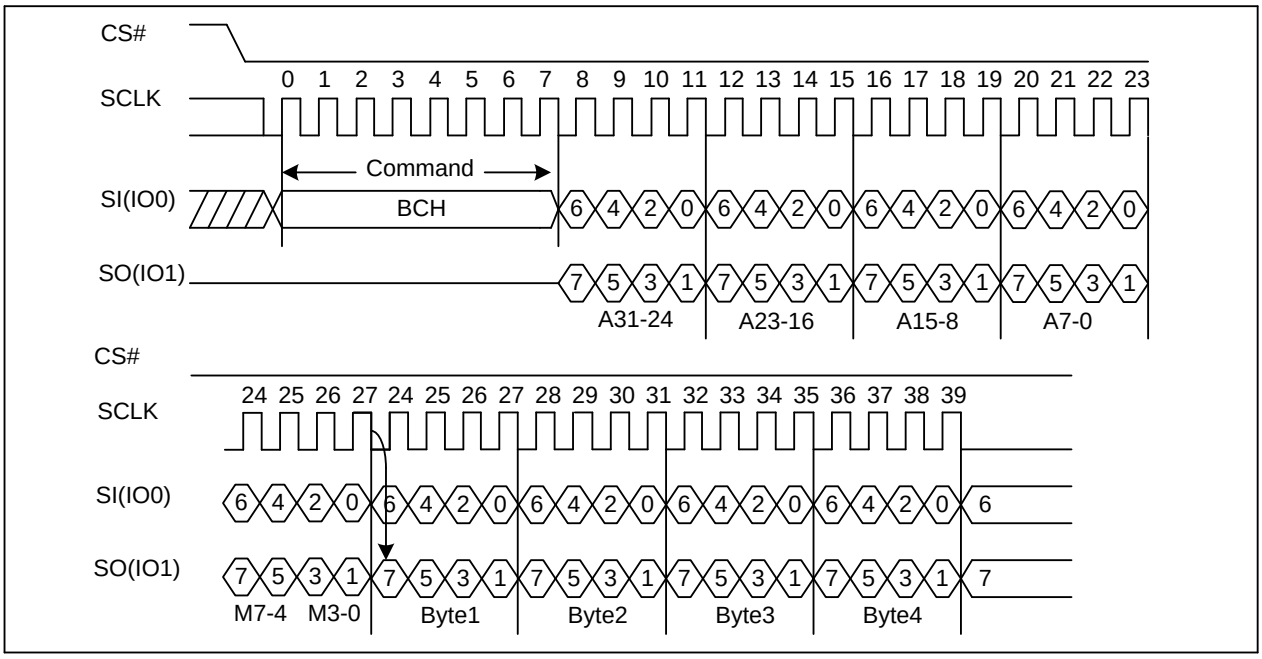
Figure 24 Dual I/O Fast Read Sequence Diagram (M5-4= (1, 0) ADS=1)



Note:

1. The dummy clock number is configurable.

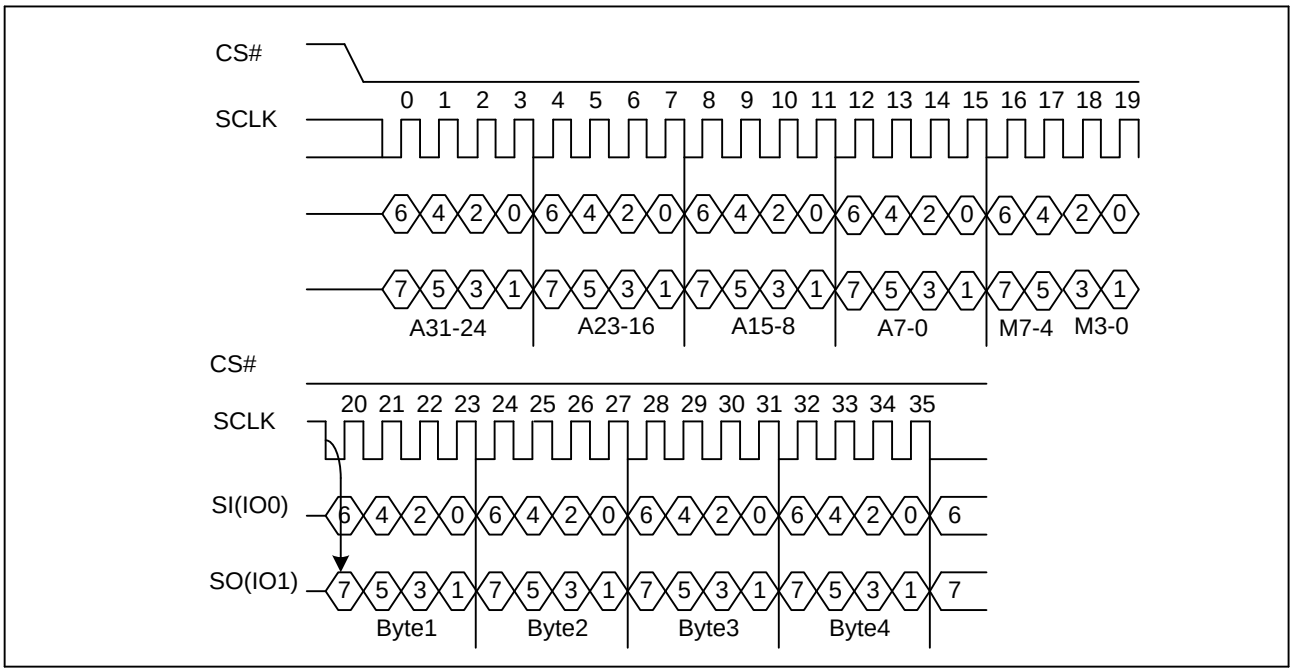
Figure 25 Dual I/O Fast Read with 4-Byte Address Sequence Diagram (M5-4≠ (1, 0), ADS=0 or ADS=1)



Note:

1. The dummy clock number is configurable.

Figure 26 Dual I/O Fast Read with 4-Byte Address Sequence Diagram (M5-4= (1, 0) ADS=0 or ADS=1)



Note:

1. The dummy clock number is configurable.

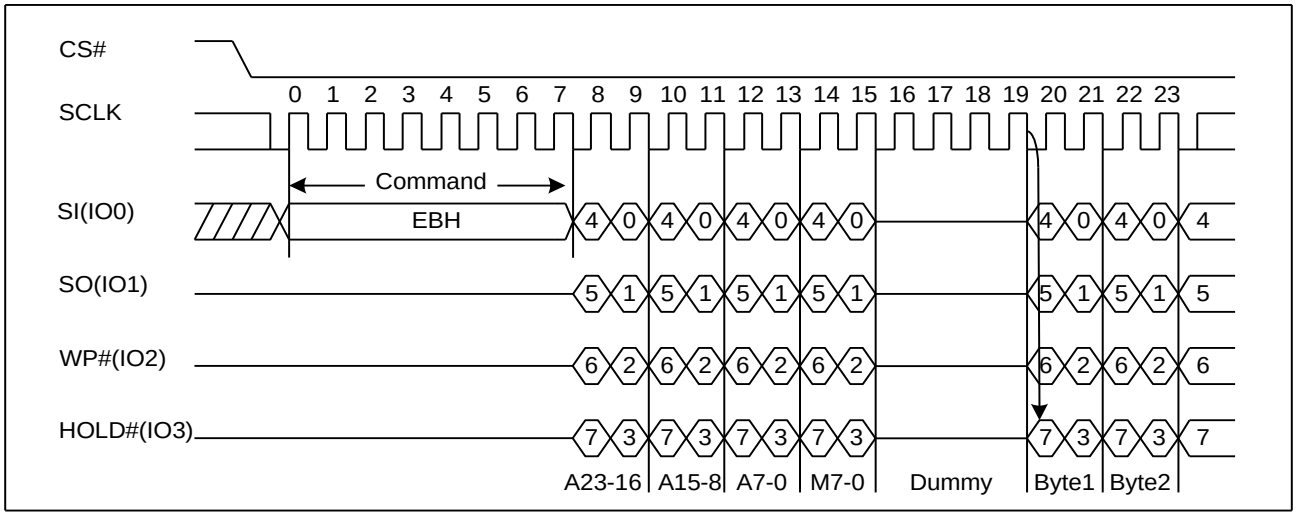
7.10. Quad I/O Fast Read (QIOFR EBH or 4QIOFR ECH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a "Continuous Read Mode" byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO2, IO3, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S6) must be set to enable for the Quad I/O Fast read command.

Quad I/O Fast Read with "Continuous Read Mode"

The Quad I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. If the "Continuous Read Mode" bits (M5-4) do not equal to (1, 0), the next command requires the first EBH command code, thus returning to normal operation. A Reset command can be used to reset (M5-4) before issuing normal command.

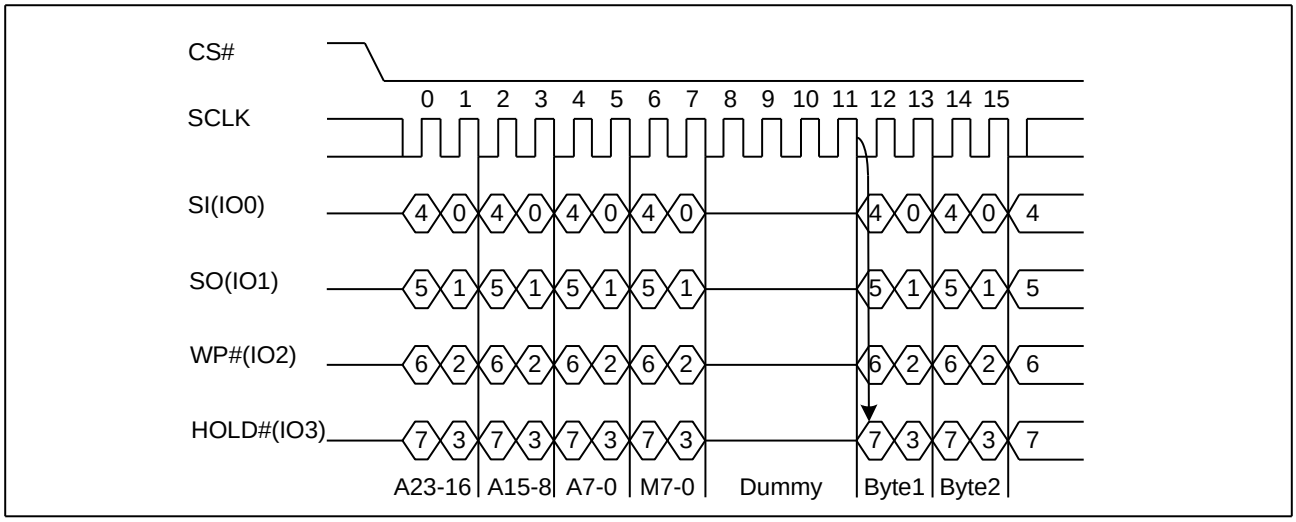
Figure 27 Quad I/O Fast Read Sequence Diagram (M5-4≠ (1, 0), ADS=0)



Note:

1. The dummy clock number is configurable.

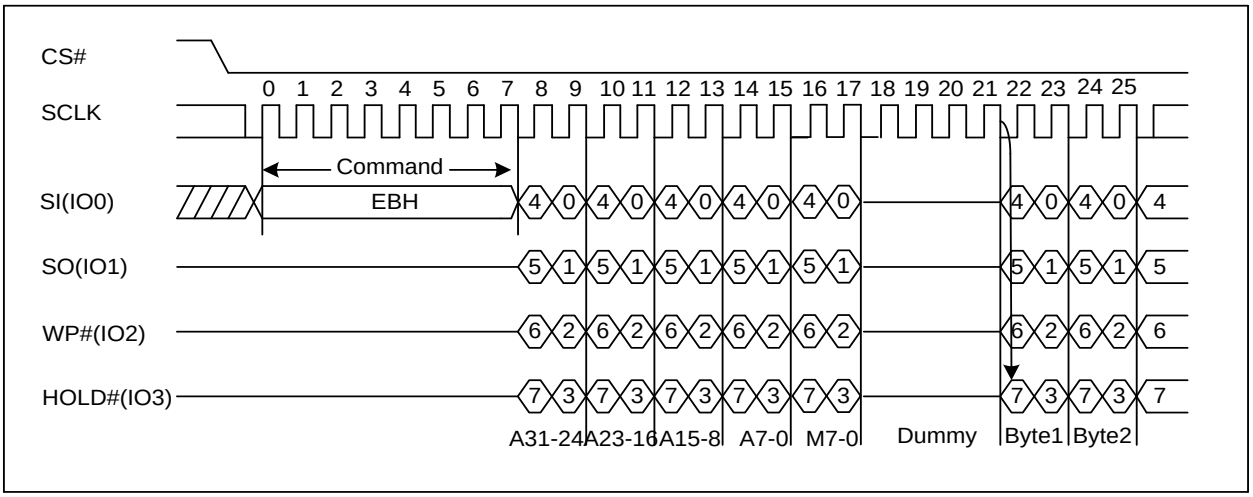
Figure 28 Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0), ADS=0)



Note:

1. The dummy clock number is configurable.

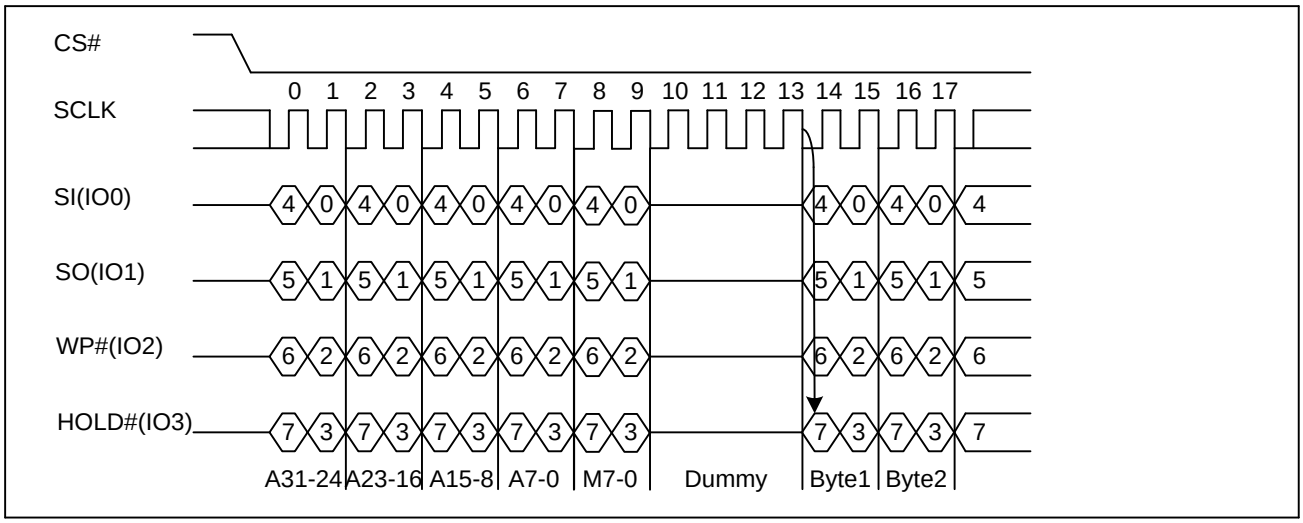
Figure 29 Quad I/O Fast Read Sequence Diagram (M5-4≠ (1, 0), ADS=1)



Note:

1. The dummy clock number is configurable.

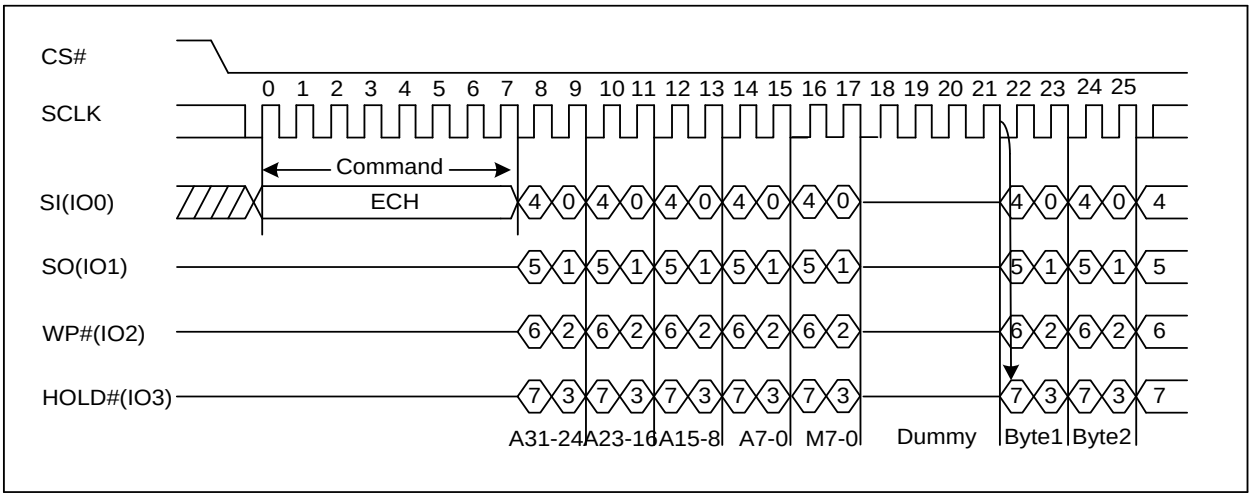
Figure 30 Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0), ADS=1)



Note:

1. The dummy clock number is configurable.

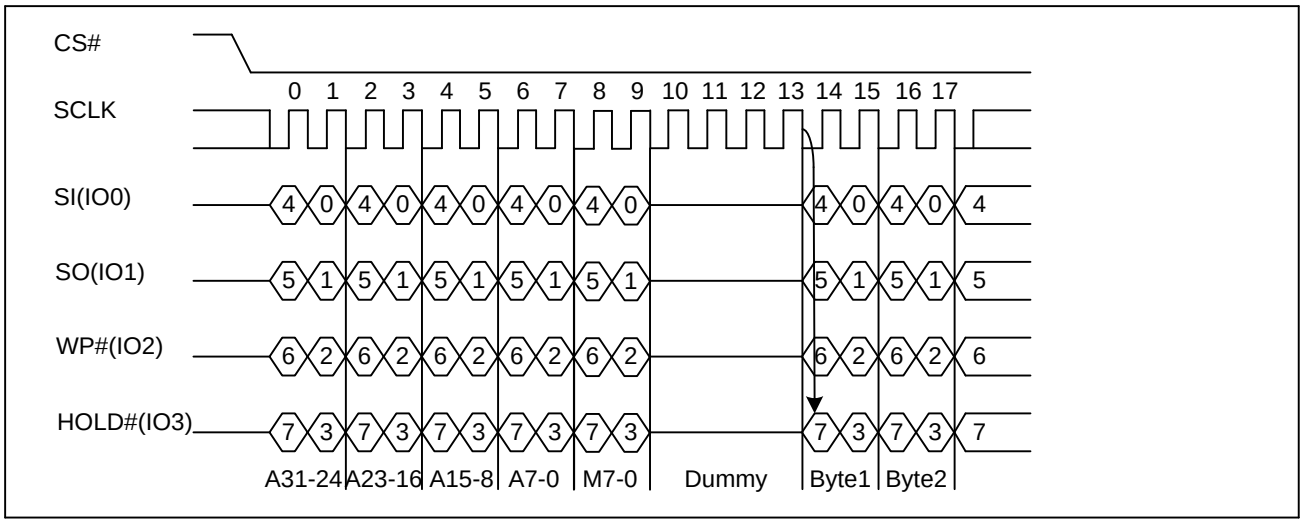
Figure 31 Quad I/O Fast Read with 4-Byte Address Sequence Diagram (M5-4≠ (1, 0), ADS=0 or ADS=1)



Note:

1. The dummy clock number is configurable.

Figure 32 Quad I/O Fast Read with 4-Byte Address Sequence Diagram (M5-4= (1, 0), ADS=0 or ADS=1)



Note:

1. The dummy clock number is configurable.

Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to EBH or ECH. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following EBH or ECH commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

7.11. Set Burst with Wrap (77H)

The Set Burst with Wrap command is used in conjunction with "Quad I/O Fast Read" command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

The Set Burst with Wrap command sequence: CS# goes low → Send Set Burst with Wrap command → Send 24 dummy bits → Send 8 bits "Wrap bits" → CS# goes high.

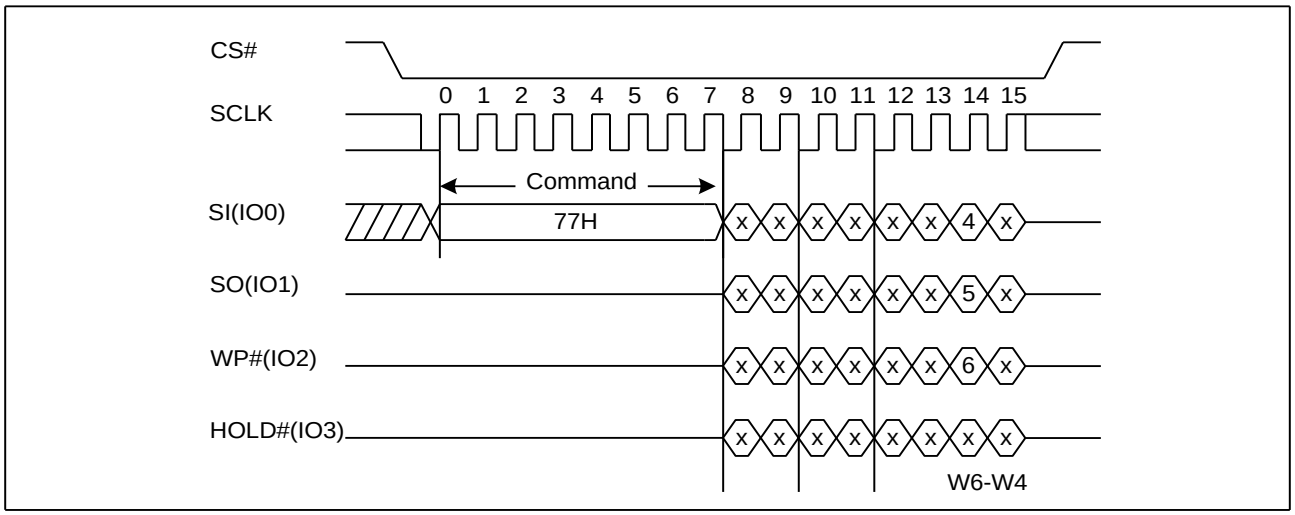
Table 16 Set Burst with Wrap configuration

W6,W5	W4=0		W4=1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0, 0	Yes	8-byte	No	N/A
0, 1	Yes	16-byte	No	N/A
1, 0	Yes	32-byte	No	N/A
1, 1	Yes	64-byte	No	N/A

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following "Quad I/O Fast Read" command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and

return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

Figure 33 Set Burst with Wrap Sequence Diagram



7.12. Page Program (PP 02H or 4PP 12H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

Figure 34 Page Program Sequence Diagram (ADS=0)

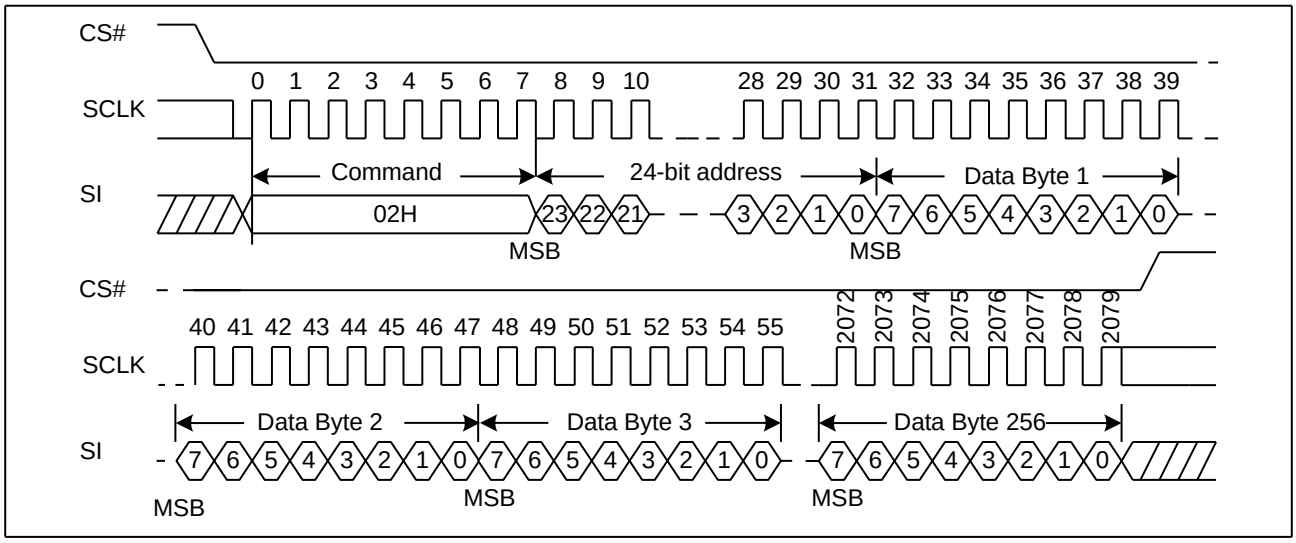


Figure 35 Page Program Sequence Diagram (ADS=1)

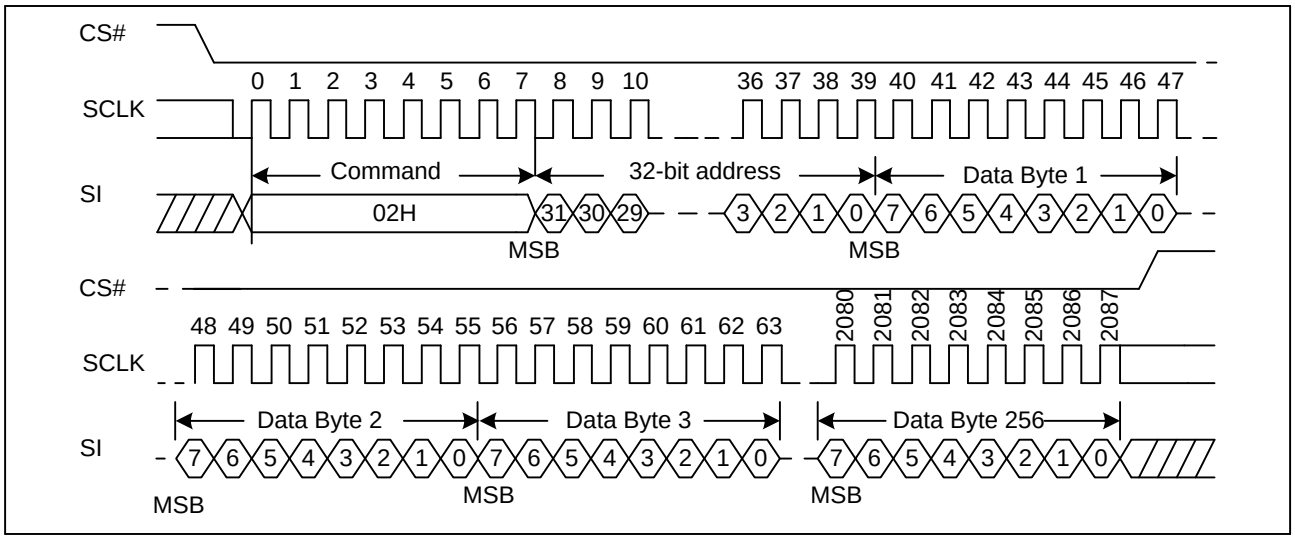
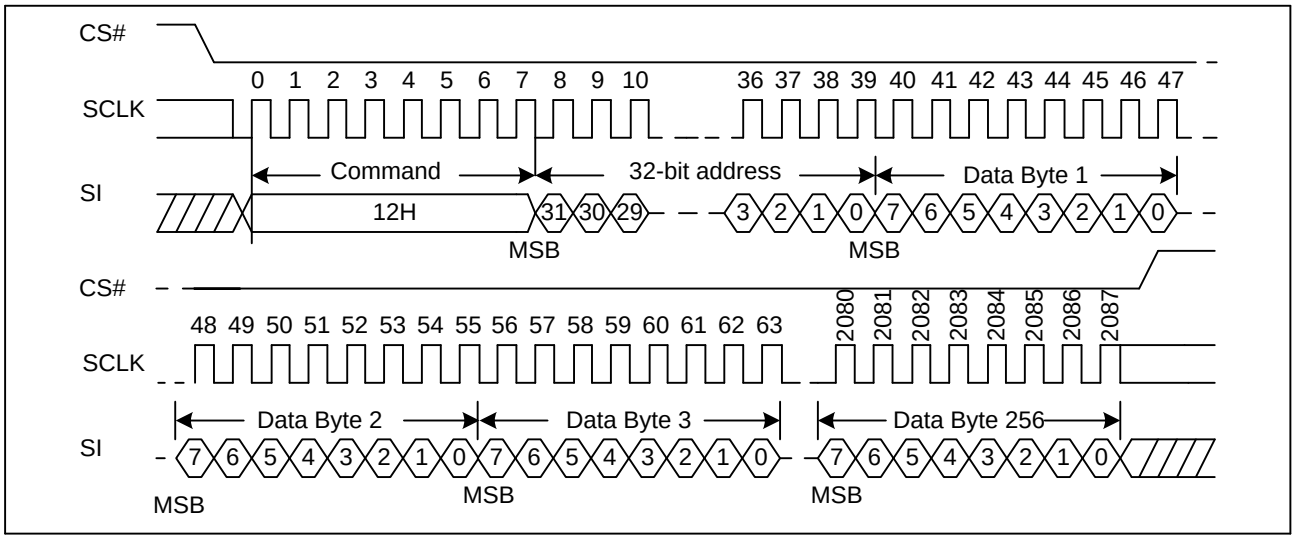


Figure 36 Page Program with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)



7.13. Quad Page Program (QPP 32H or 4QPP 3EH)

The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. To use Quad Page Program the Quad enable in status register Bit6 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address bytes and at least one data byte on IO pins.

The command sequence is shown below. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is t_{PP}) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

Figure 37 Quad Page Program Sequence Diagram (ADS=0)

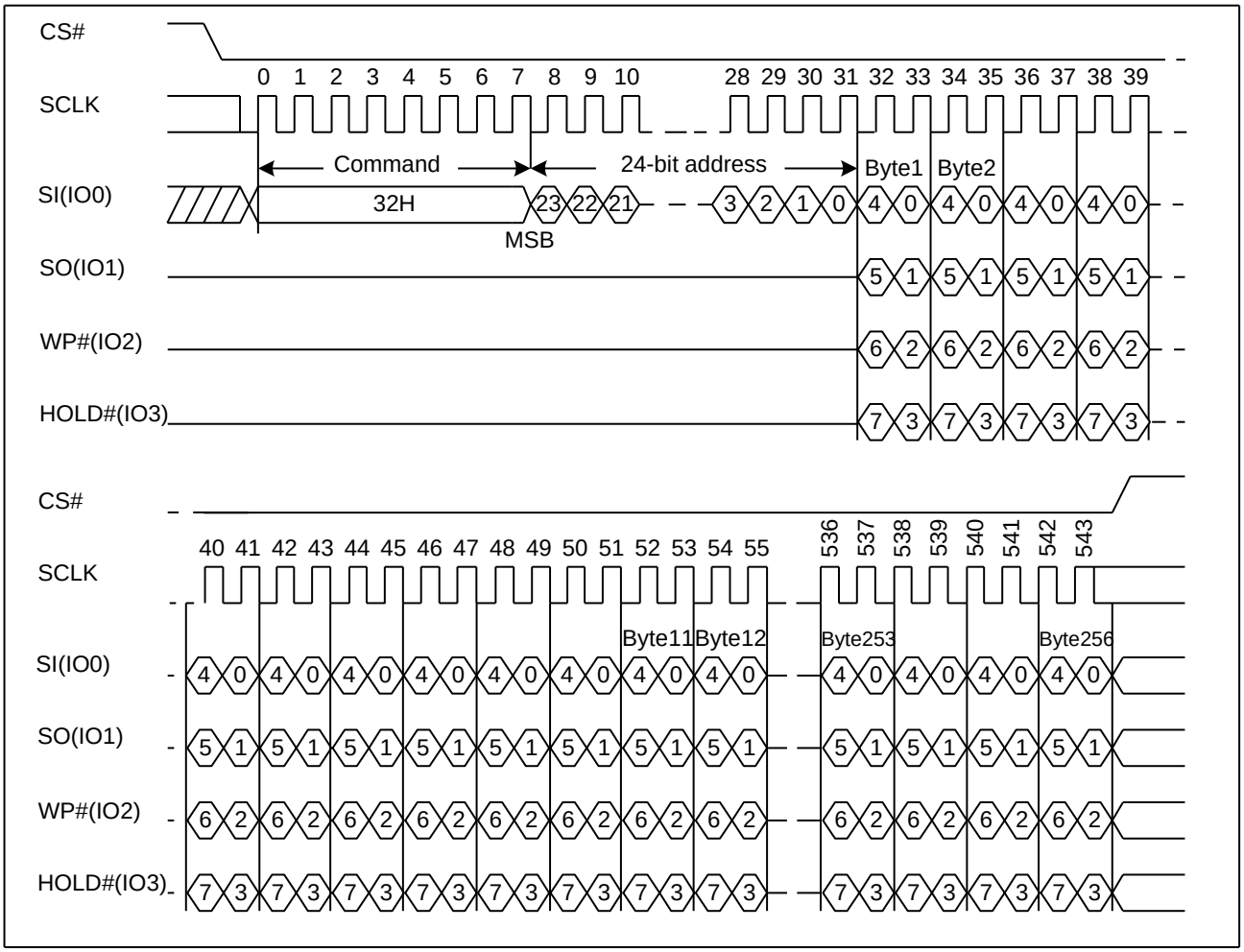


Figure 38 Quad Page Program Sequence Diagram (ADS=1)

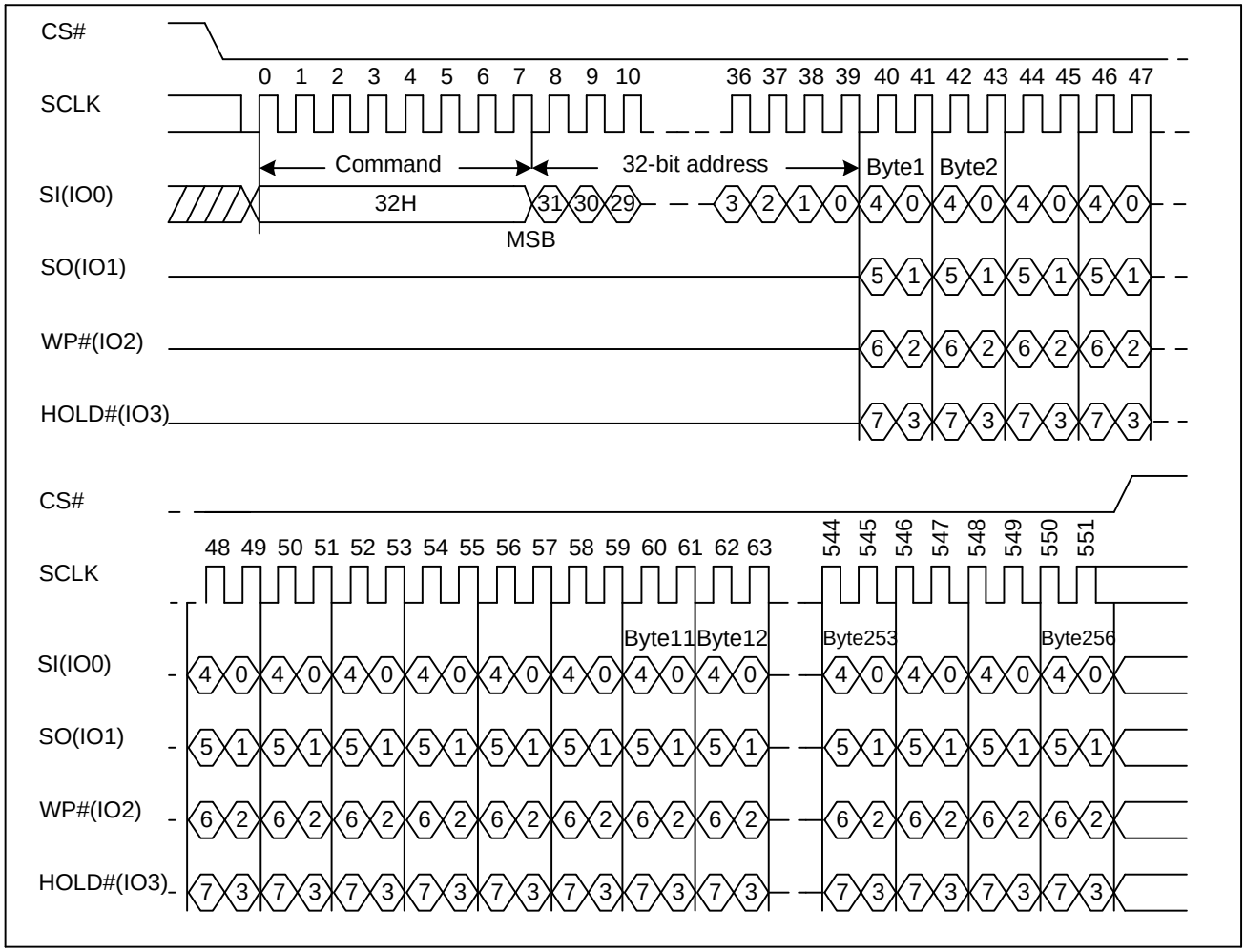
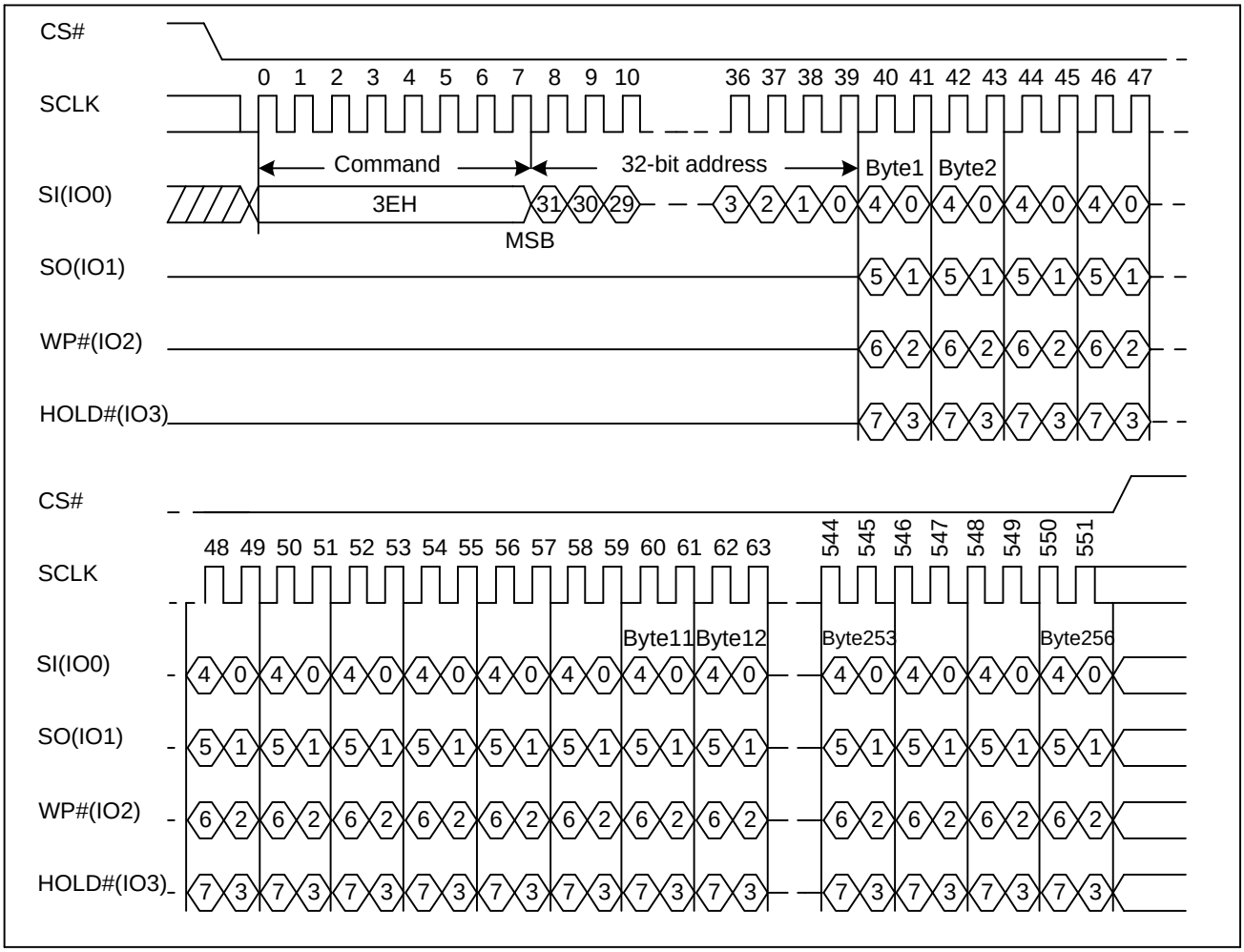


Figure 39 Quad Page Program with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)



7.14. Sector Erase (SE 20H or 4SE 21H)

The Sector Erase (SE) command is erased the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bit is not executed.

Figure 40 Sector Erase Sequence Diagram (ADS=0)

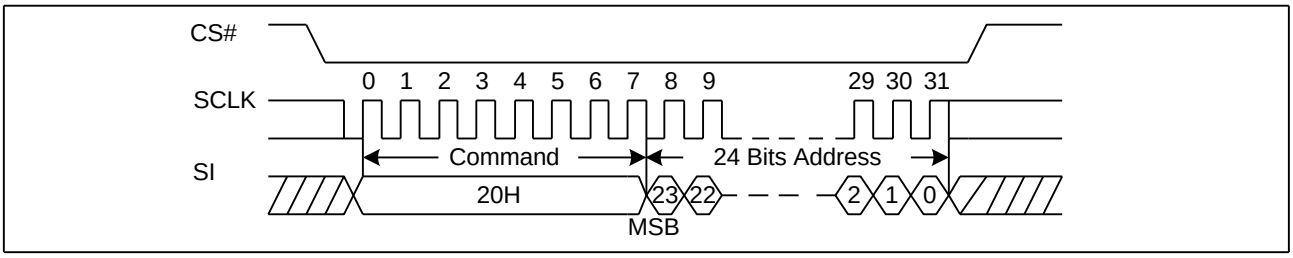


Figure 41 Sector Erase Sequence Diagram (ADS=1)

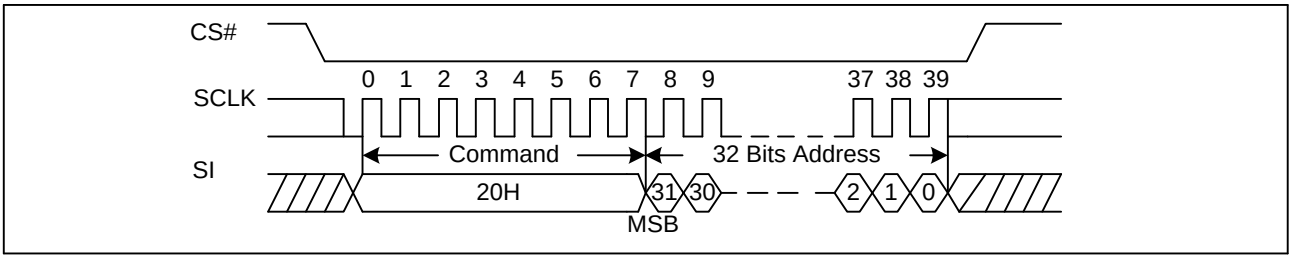
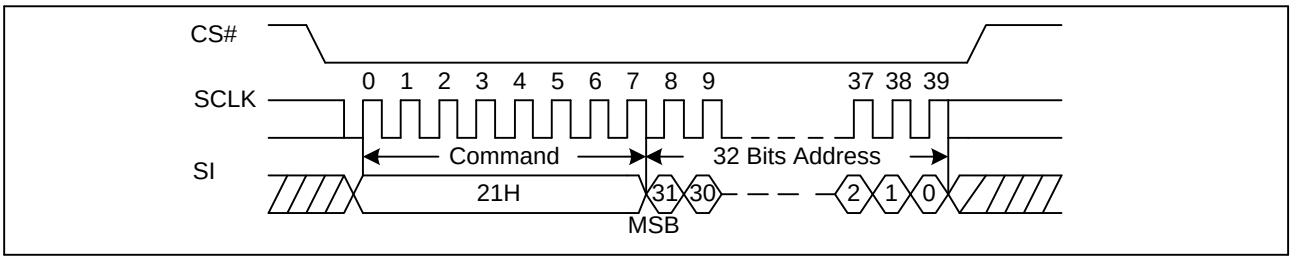


Figure 42 Sector Erase with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)



7.15. 32KB Block Erase (BE32 52H or 4BE32 5CH)

The 32KB Block Erase (BE) command is erased the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits is not executed.

Figure 43 32KB Block Erase Sequence Diagram (ADS=0)

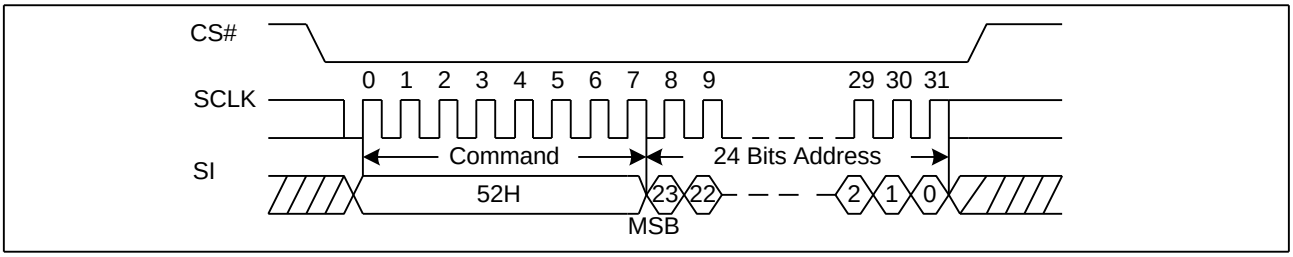


Figure 44 32KB Block Erase Sequence Diagram (ADS=1)

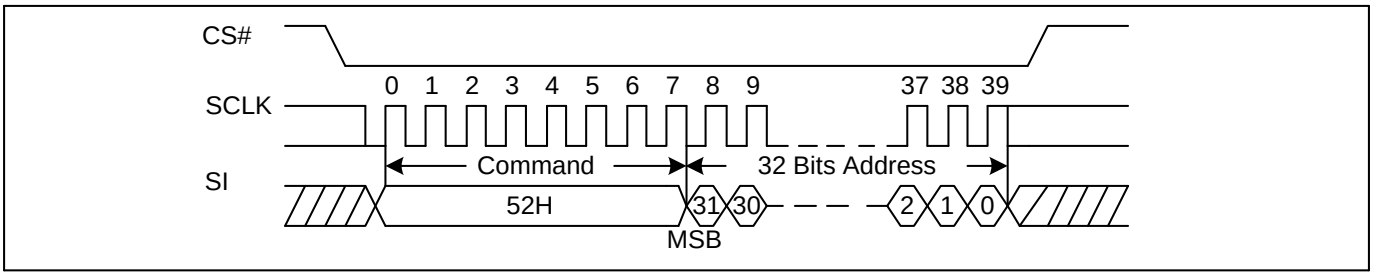
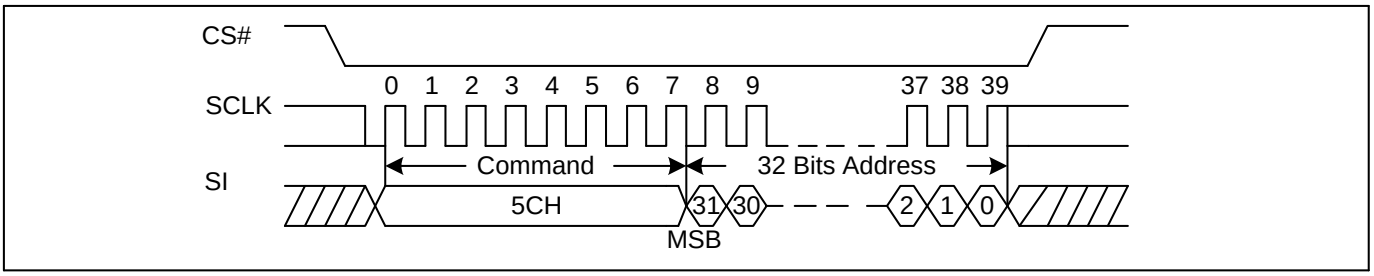


Figure 45 32KB Block Erase with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)



7.16. 64KB Block Erase (BE64 D8H or 4BE64 DCH)

The 64KB Block Erase (BE) command is erased the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command → 3-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits is not executed.

Figure 46 64KB Block Erase Sequence Diagram (ADS=0)

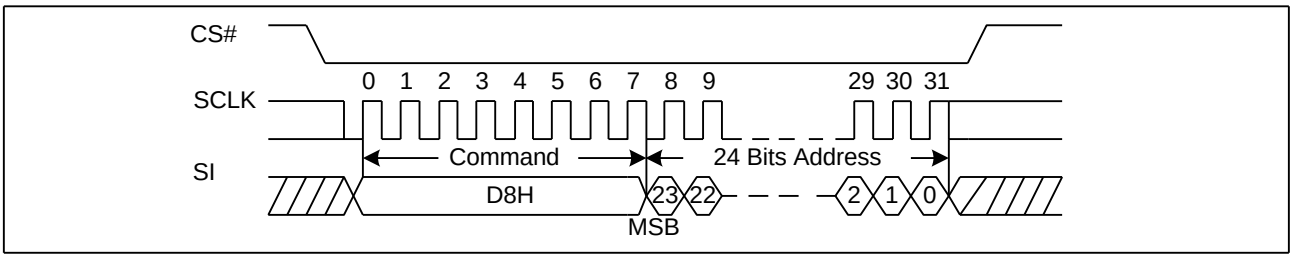


Figure 47 64KB Block Erase Sequence Diagram (ADS=1)

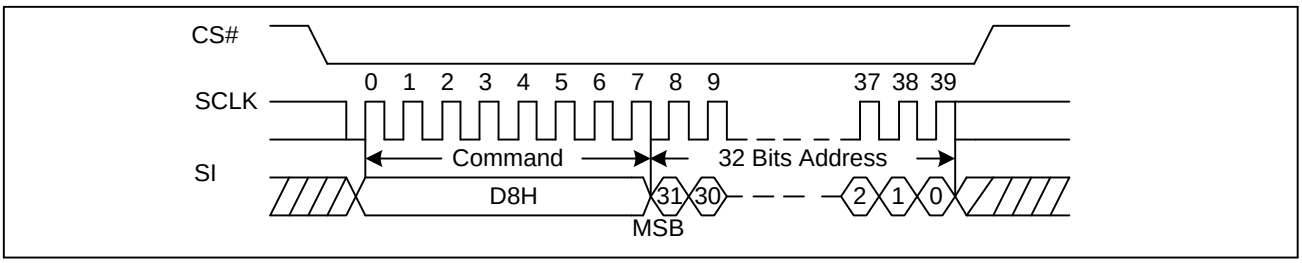
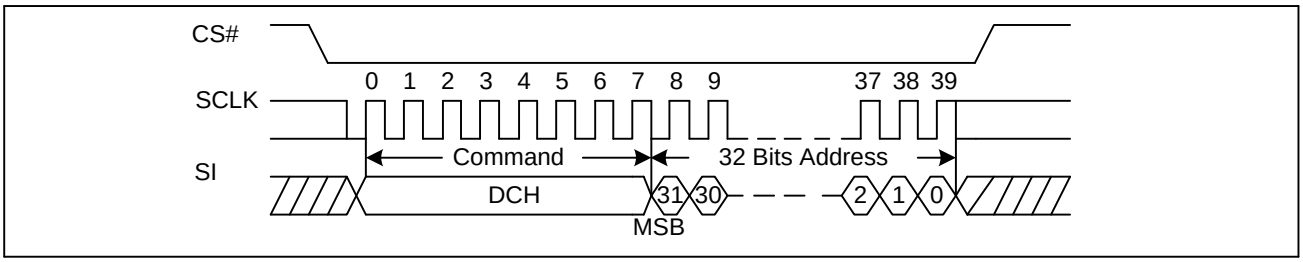


Figure 48 64KB Block Erase with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)

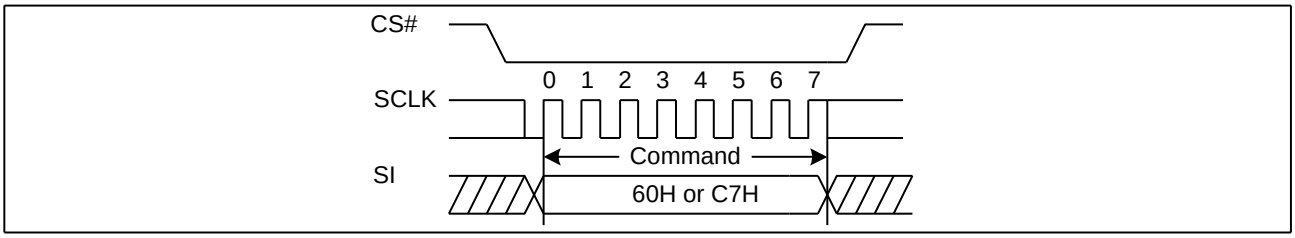


7.17. Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is erased the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is ignored if one or more sectors/blocks are protected.

Figure 49 Chip Erase Sequence Diagram



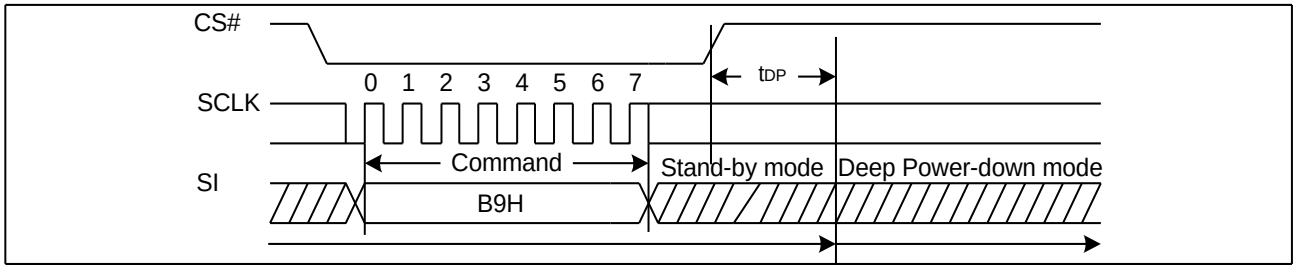
7.18. Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command. This releases the device from this mode. The Release from Deep Power-Down and Read Device ID (RDI) command also allows the Device ID of the device to be output on SO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always Power-Up in the Standby Mode. The Deep Power-Down (DP) command is entered by driving CS# low, followed by the command code on SI. CS# must be driven low for the entire duration of the sequence.

The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 50 Deep Power-Down Sequence Diagram



7.19. Read Unique ID (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence in 3 byte mode (ADS=0): CS# goes low → sending Read Unique ID command →Dummy Byte1 →Dummy Byte2 →Dummy Byte3 →Dummy Byte4→128bit Unique ID Out →CS# goes high.

The Read Unique ID command sequence in 4 byte mode (ADS=0): CS# goes low → sending Read Unique ID command →Dummy Byte1 →Dummy Byte2 →Dummy Byte3 →Dummy Byte4→ Dummy Byte5→128bit Unique ID Out →CS# goes high.

Figure 51 Read Unique ID Sequence Diagram (ADS=0)

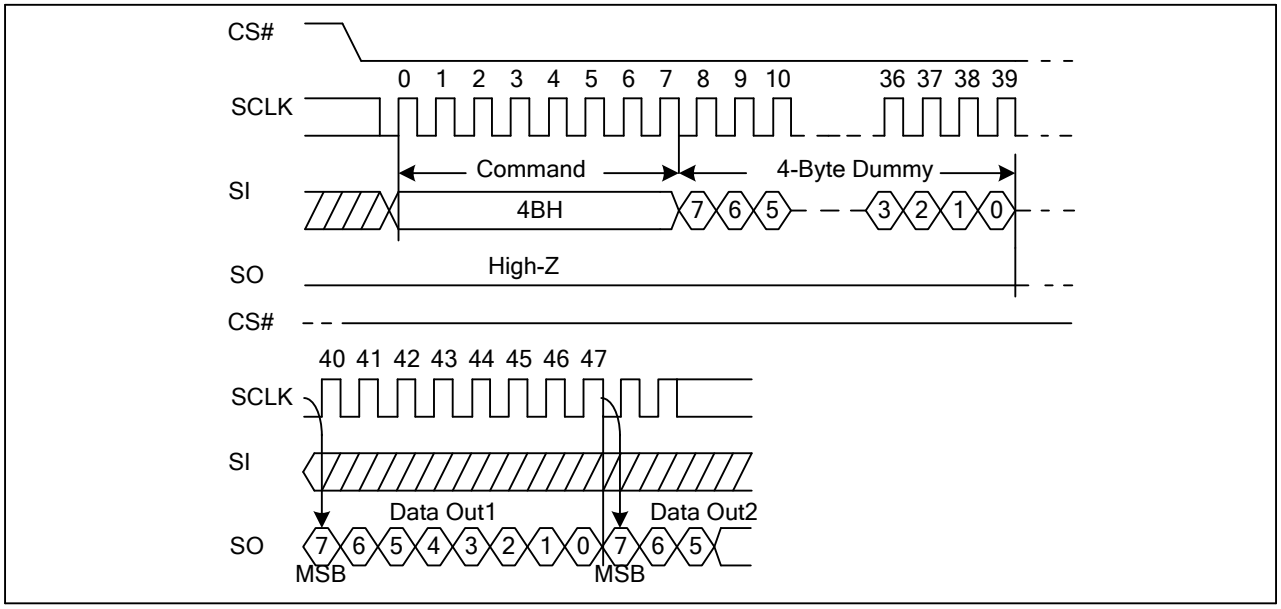
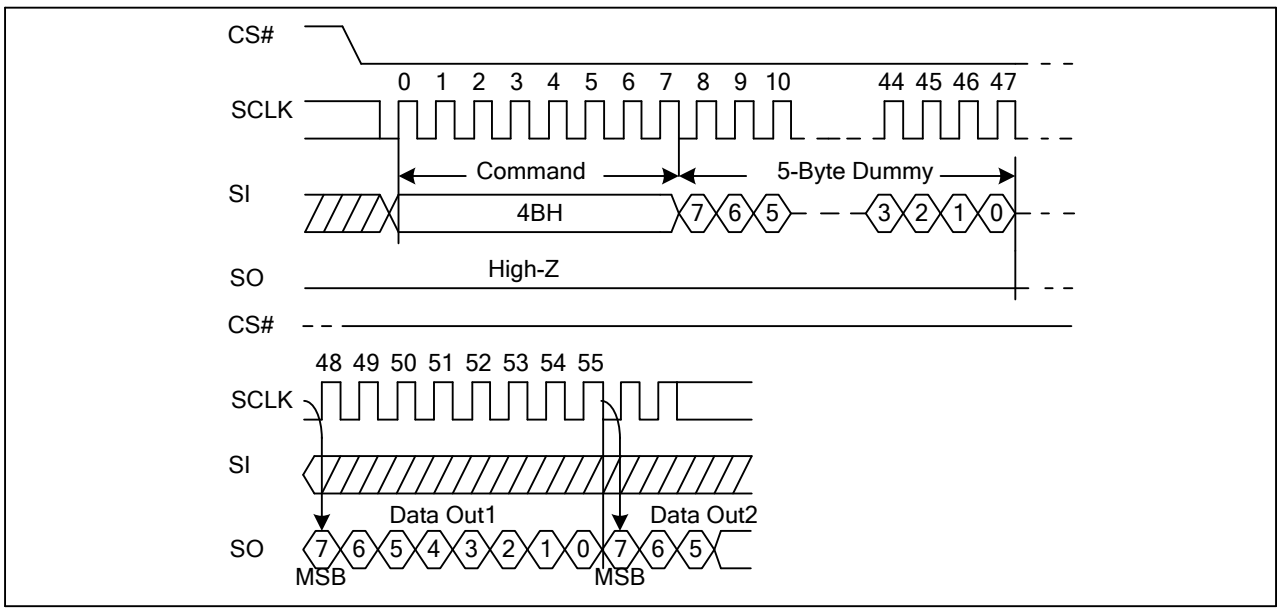


Figure 52 Read Unique ID Sequence Diagram (ADS=1)



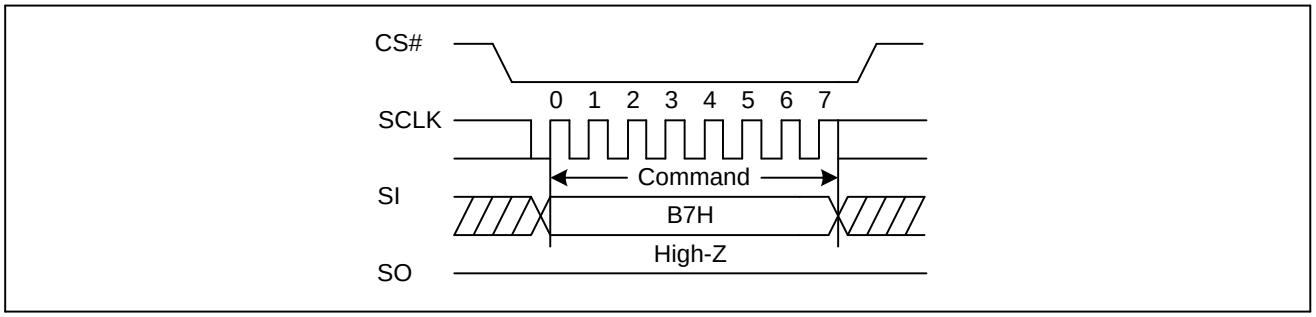
7.20. Enter 4-Byte Address Mode (B7H)

The Enter 4-byte Address Mode command enables accessing the address length of 32-bit for the memory area of higher density (larger than 128Mb). The device default is in 24-bit address mode; after sending out the EN4B instruction, the bit13 (ADS bit) of status register will be automatically set to "1" to indicate the 4-byte address mode has been enabled. Once the 4-byte address mode is enabled, the address length becomes 32-bit instead of the default 24-bit.

All instructions are accepted normally, and just the address bit is changed from 24-bit to 32-bit.

The sequence of issuing EN4B instruction is: CS# goes low → sending Enter 4-byte mode command →CS# goes high.

Figure 53 Enter 4-Byte Address Mode Sequence Diagram

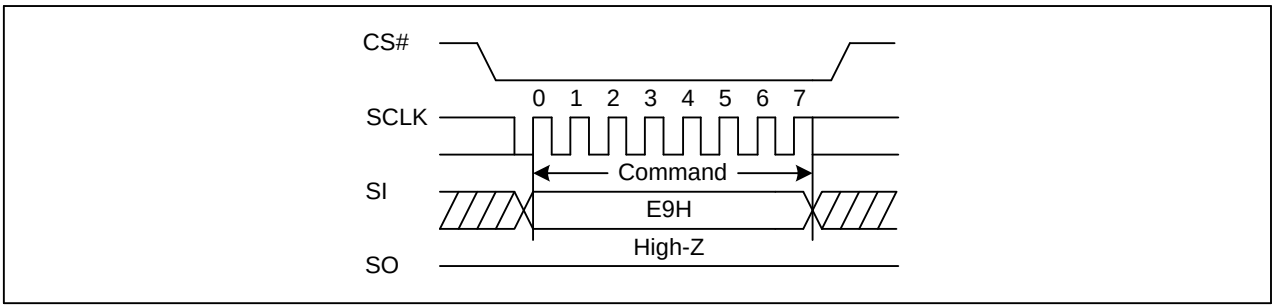


7.21. Exit 4-Byte Address Mode (E9H)

The Exit 4-byte Address Mode command is executed to exit the 4-byte address mode and return to the default 3-byte address mode. After sending out the EX4B instruction, the bit13 (ADS bit) of status register will be cleared to "0" to indicate the exit of the 4-byte address mode. Once exiting the 4-byte address mode, the address length will return to 24-bit.

The sequence of issuing EN4B instruction is: CS# goes low → sending Exit 4-byte Address Mode command →CS# goes high.

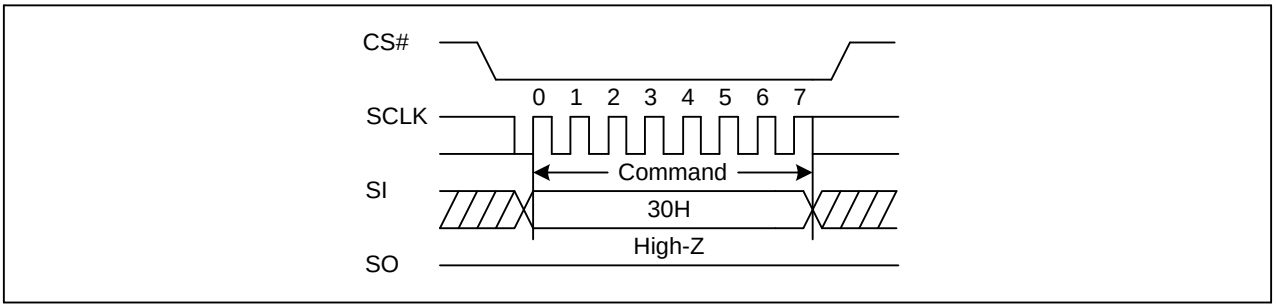
Figure 54 Exit 4-Byte Address Mode Sequence Diagram



7.22. Clear SR Flags (30H)

The Clear Status Register Flags command resets bit S21 (Program Error bit) and S22 (Erase Error bit) from status register. It is not necessary to set the WEL bit before the Clear Status Register command is executed. The Clear SR command will be accepted even when the device remains busy with WIP set to 1, as the device does remain busy when either error bit is set. The WEL bit will be unchanged after this command is executed.

Figure 55 Clear Status Register Flags Sequence Diagram



7.23. Release from Deep Power-Down and Read Device ID (RDI) (ABH)

The Release from Power-Down and Read Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code "ABH" and driving CS# high as shown below. Release from Power-Down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code "ABH" followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown below. The Device ID value for the GD25Q512MC is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not have any effects on the current cycle.

Figure 56 Release Power-Down Sequence Diagram

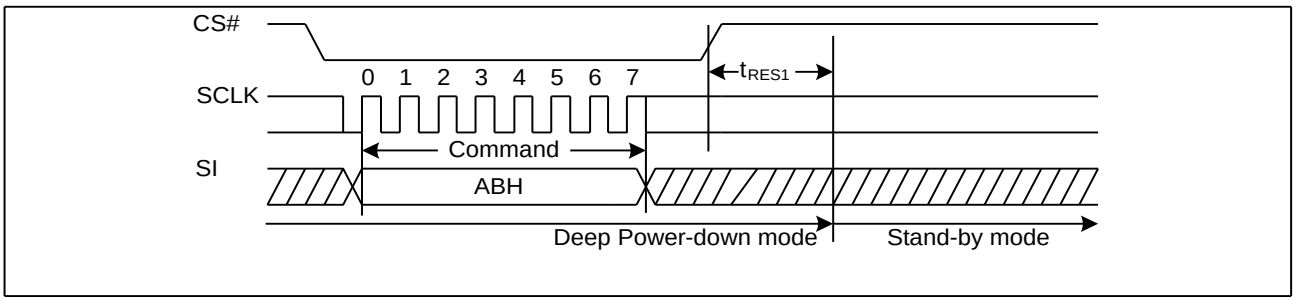
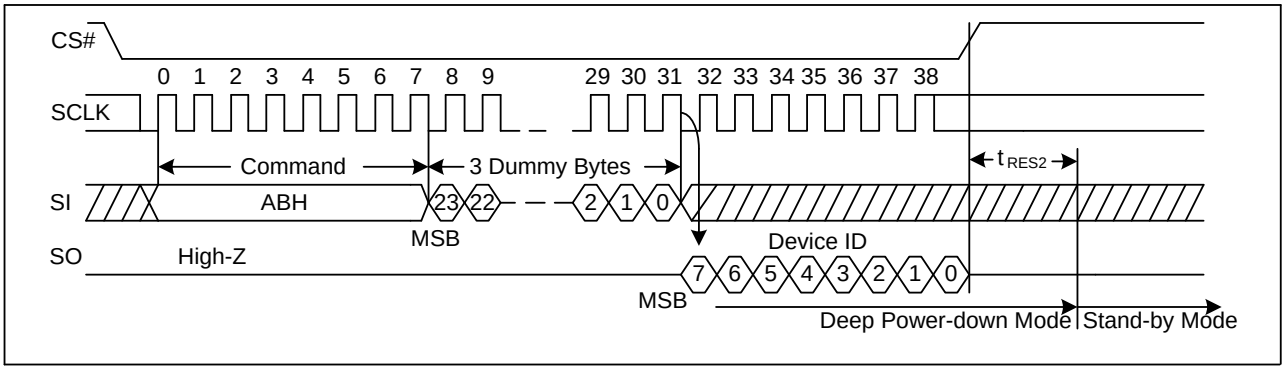


Figure 57 Release Power-Down/Read Device ID Sequence Diagram

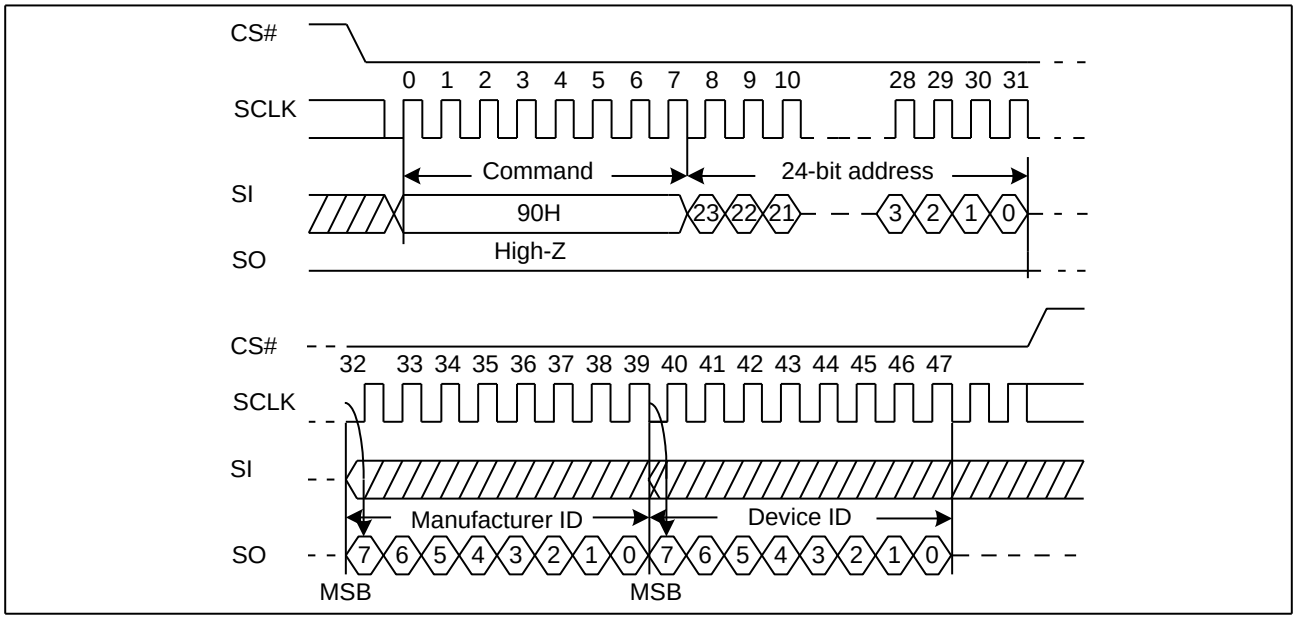


7.24. Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code "90H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown below.

Figure 58 Read Manufacture ID/ Device ID Sequence Diagram

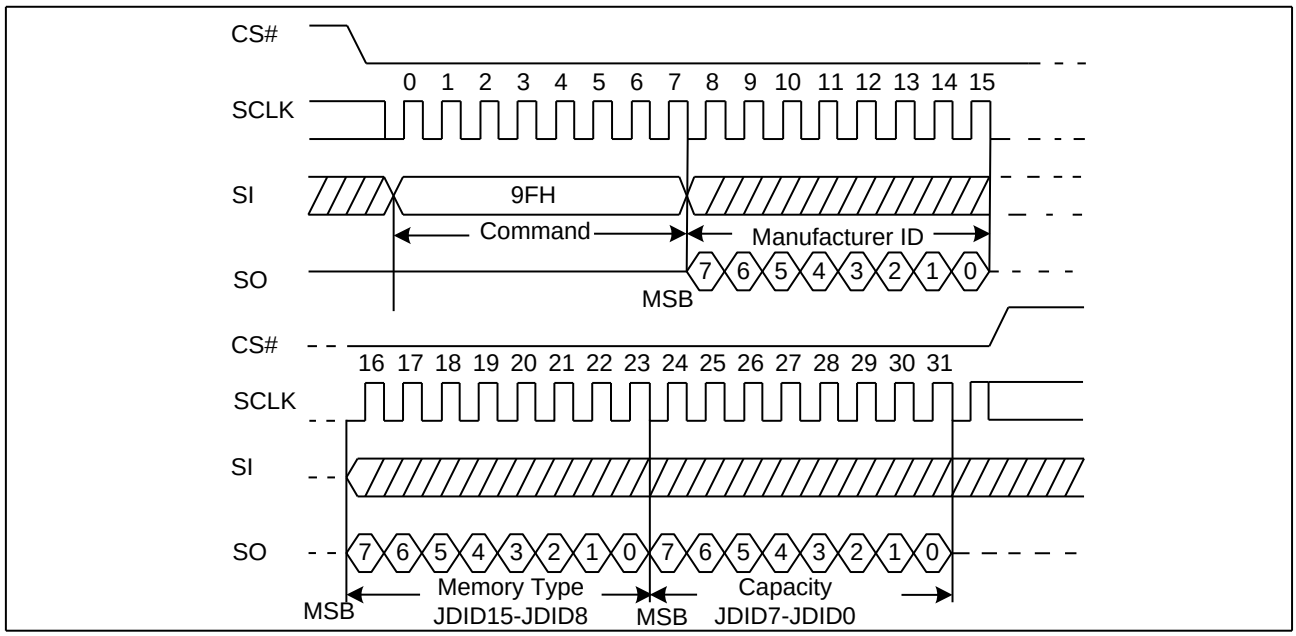


7.25. Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. The Read Identification (RDID) command while an Erase or Program cycle is in progress is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure 59 Read Identification ID Sequence Diagram



7.26. Program/Erase Suspend (PES) (75H)

The Program/Erase Suspend command "75H", allows the system to interrupt a page program or sector/block erase operation and then read data from any other sector or block. The Write Status Register command (01H/31H/11H) and Erase commands (20H, 52H, D8H, C7H, 60H) and Page Program command (02H / 32H) are not allowed during Program/Erase suspend. Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of "tsus" (See AC Characteristics) is required to suspend the program/erase operation.

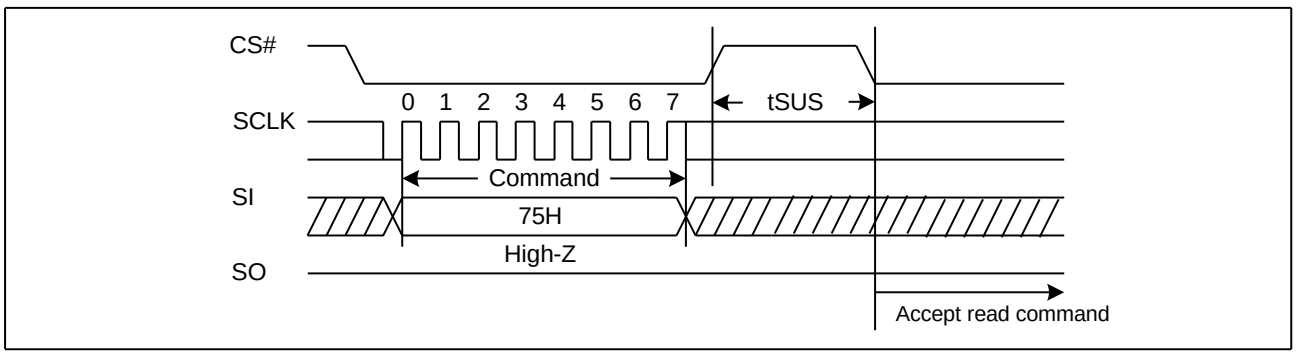
Table 17 Commands Allowed During Program or Erase Suspend

Command Name	Code (Hex)	Allowed During Erase Suspend	Allowed During Program Suspend	Comment
Write Enable	06	Yes		Required for program command within erase suspend.
Read Status Register-1	05	Yes	Yes	Needed to read WIP to determine end of suspend process.
Read Status Register-2	35	Yes	Yes	Needed to read suspend status to determine whether the operation is suspended or complete.
Read Status Register-3	15	Yes	Yes	Needed to read suspend status to determine whether the operation is suspended or complete.
Read Extended Addr. Register	C8	Yes	Yes	Extended Addr. Register may need to be changed during a suspend to reach a sector needed for read or program.

Write Extended Addr. Register	C5	Yes	Yes	Extended Addr. Register may need to be changed during a suspend to reach a sector needed for read or program.
Read	03	Yes	Yes	All array reads allowed in suspend.
4Read	13	Yes	Yes	All array reads allowed in suspend.
Fast Read	0B	Yes	Yes	All array reads allowed in suspend.
4Fast Read	0C	Yes	Yes	All array reads allowed in suspend.
Dual I/O Fast Read	BB	Yes	Yes	All array reads allowed in suspend.
4Dual I/O Fast Read	BC	Yes	Yes	All array reads allowed in suspend.
Dual Output Fast Read	3B	Yes	Yes	All array reads allowed in suspend.
4Dual Output Fast Read	3C	Yes	Yes	All array reads allowed in suspend.
Quad I/O Fast Read	EB	Yes	Yes	All array reads allowed in suspend.
4Quad I/O Fast Read	EC	Yes	Yes	All array reads allowed in suspend.
Quad Output Fast Read	6B	Yes	Yes	All array reads allowed in suspend.
4Quad Output Fast Read	6C	Yes	Yes	All array reads allowed in suspend.
Page Program	02	Yes		Required for array program during erase suspend.
4Page Program	12	Yes		Required for array program during erase suspend.
Quad Page Program	32	Yes		Required for array program during erase suspend.
4Quad Page Program	3E	Yes		Required for array program during erase suspend.
Program/Erase Suspend	75	Yes		Program suspend allowed during erase suspend.
Program/Erase Resume	7A	Yes		Required to resume from erase/program suspend.
Enable Reset	66	Yes	Yes	Reset allowed anytime.
Reset	99	Yes	Yes	Reset allowed anytime.

The Program/Erase Suspend command will be accepted by the device only if the SUS_P/SUS_E bit in the Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS_P/SUS_E bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within “tsus” and the SUS_P/SUS_E bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state.

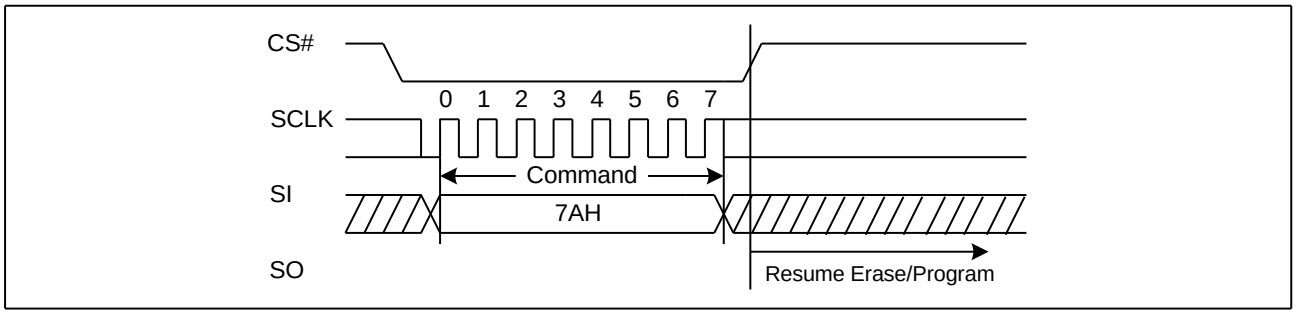
Figure 60 Program/Erase Suspend Sequence Diagram



7.27. Program/Erase Resume (PER) (7AH)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase command will be accepted by the device only if the SUS_P/SUS_E bit equal to 1 and the WIP bit equal to 0. After issued the SUS_P/SUS_E bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active.

Figure 61 Program/Erase Resume Sequence Diagram



7.28. Erase Security Registers (44H)

The GD25Q512MC provides three 512-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → sending Erase Security Registers command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is t_{SE}) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB3-1) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Table 18 Security Registers

Address	A23-16	A15-12	A11-8	A7-0
Security Register #1	00H	0 0 0 1	0 0 0 0	Do not care
Security Register #2	00H	0 0 1 0	0 0 0 0	Do not care
Security Register #3	00H	0 0 1 1	0 0 0 0	Do not care

Figure 62 Erase Security Registers command Sequence Diagram (ADS=0)

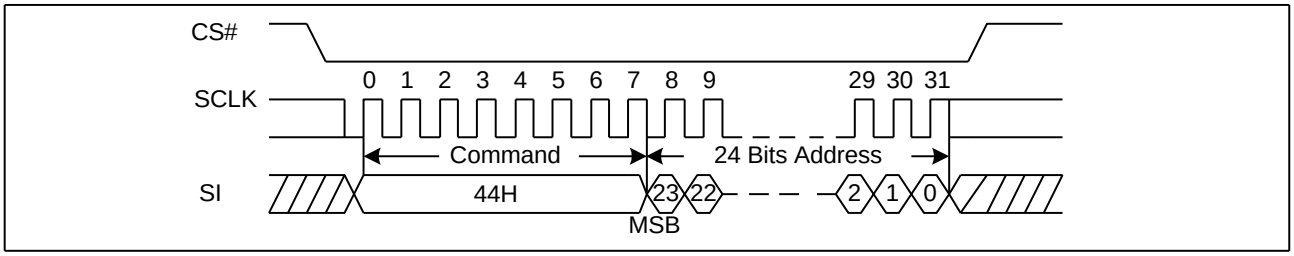
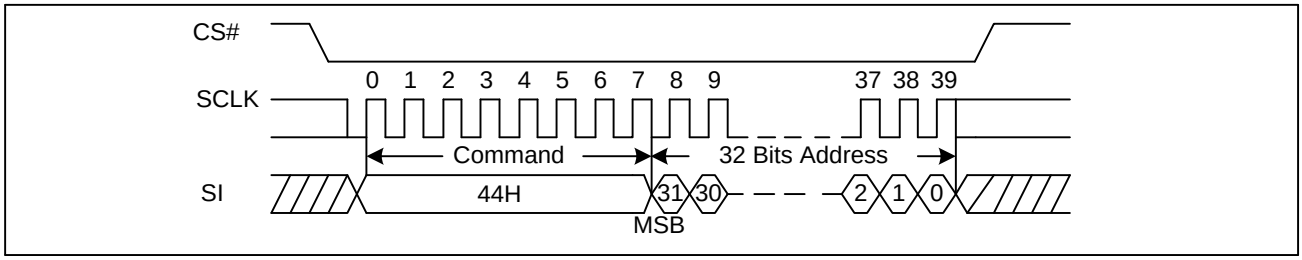


Figure 63 Erase Security Registers command Sequence Diagram (ADS=1)



7.29. Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 256 bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is t_{PP}) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB3-1) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Table 19 Security Registers

Address	A23-16	A15-12	A11-8	A7-0
Security Register #1	00H	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00H	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00H	0 0 1 1	0 0 0 0	Byte Address

Figure 64 Program Security Registers command Sequence Diagram (ADS=0)

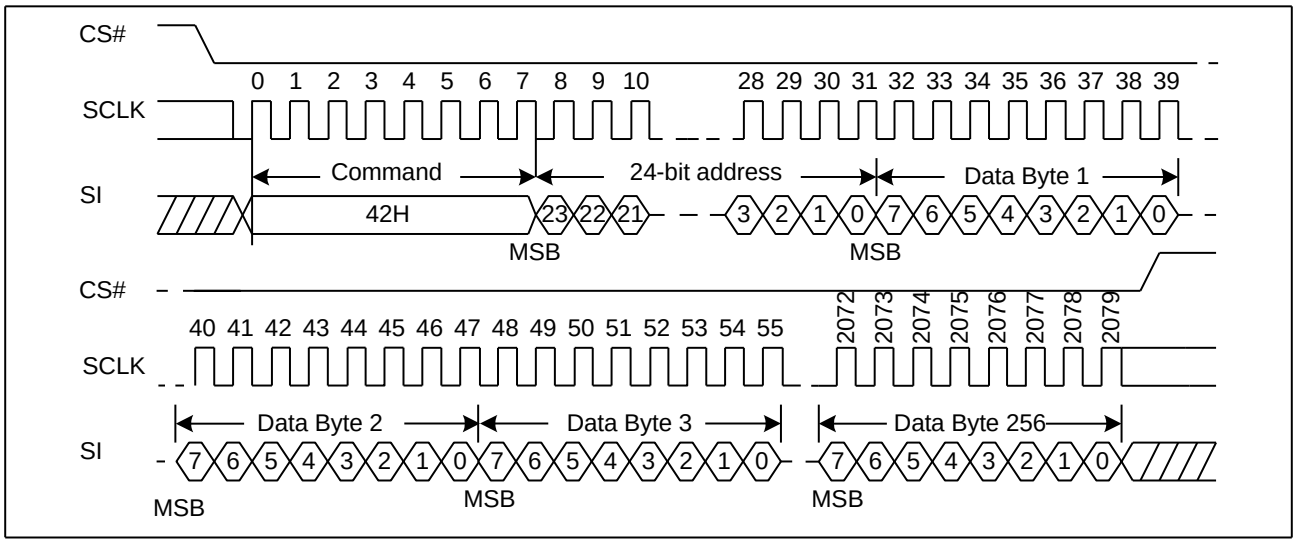
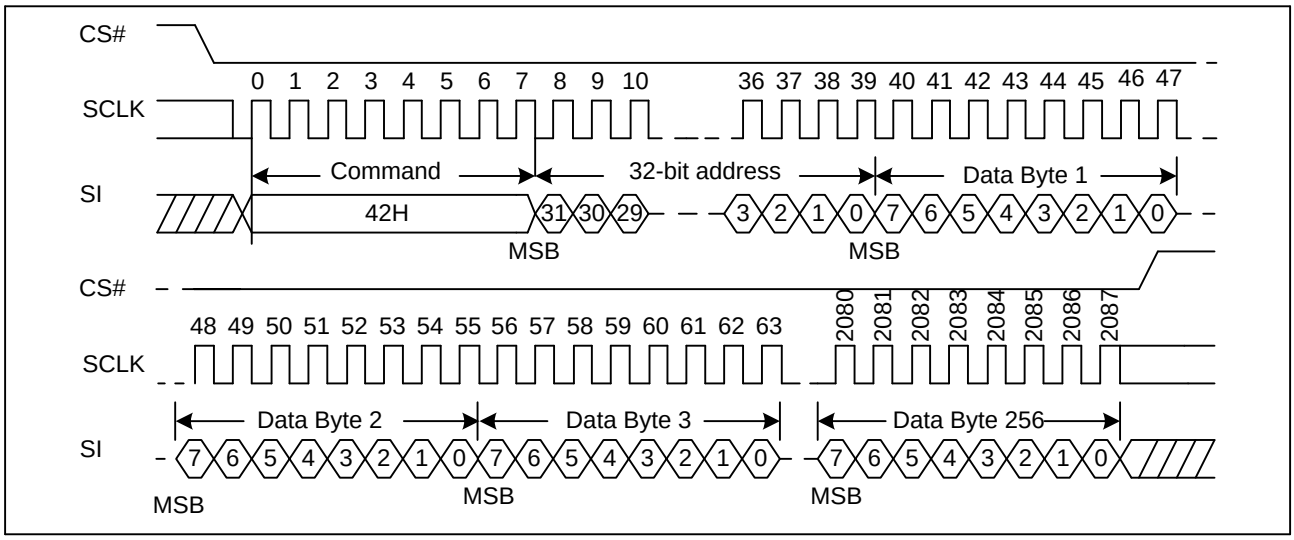


Figure 65 Program Security Registers command Sequence Diagram (ADS=1)


CS#
SCLK
SI
0 1 2 3 4 5 6 7 8 9 10
36 37 38 39 40 41 42 43 44 45 46 47
Command
32-bit address
Data Byte 1
42H
31 30 29
3 2 1 0 7 6 5 4 3 2 1 0
MSB
MSB
CS#
SCLK
SI
48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
2080 2081 2082 2083 2084 2085 2086 2087
Data Byte 2
Data Byte 3
Data Byte 256
7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0
MSB
MSB
MSB

7.30. Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command i is followed by a 3-byte address (A23-A0) or 4-byte address (A31-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_C, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A7-A0 address reaches the last byte of the register (Byte 0FFH), it will reset to 000H, the command is completed by driving CS# high.

Table 20 Security Registers

Address	A23-16	A15-12	A11-8	A7-0
Security Register #1	00H	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00H	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00H	0 0 1 1	0 0 0 0	Byte Address

Figure 66 Read Security Registers command Sequence Diagram (ADS=0)

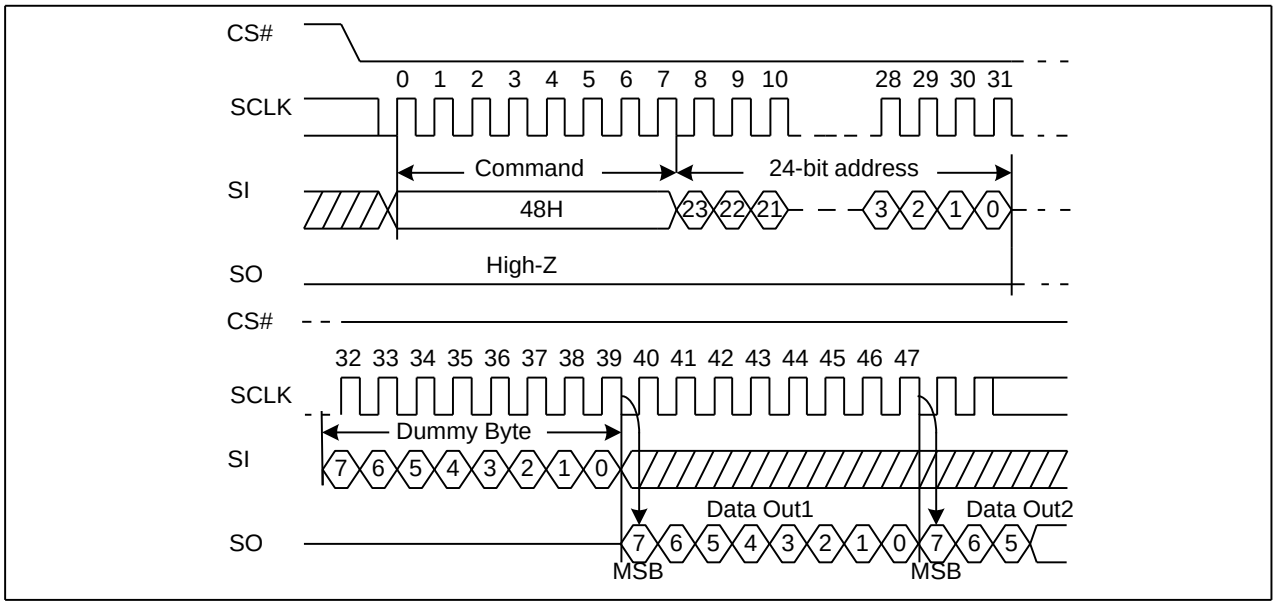
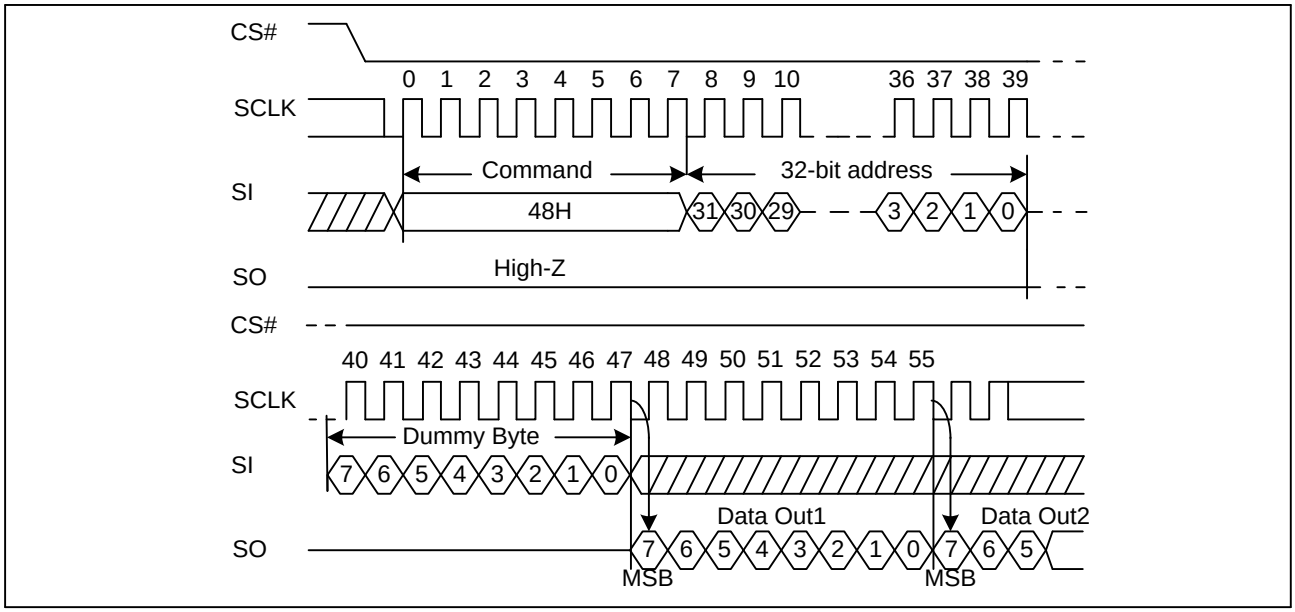


Figure 67 Read Security Registers command Sequence Diagram (ADS=1)

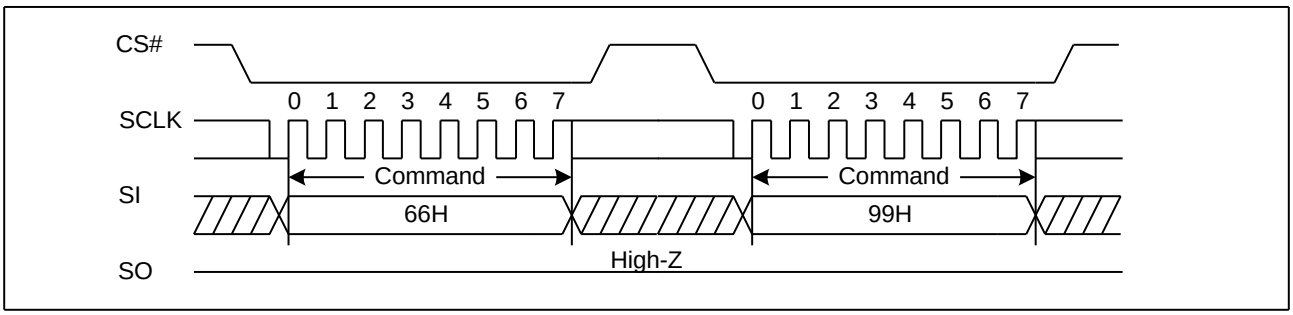


7.31. Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Suspend status, Continuous Read Mode bit setting (M7-M0) and Wrap Bit Setting (W6-W4).

The "Enable Reset (66H)" and the "Reset (99H)" commands can be issued in SPI mode. The "Reset (99H)" command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately t_{RST} =60us to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

Figure 68 Enable Reset and Reset command Sequence Diagram



7.32. Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

Figure 69 Read Serial Flash Discoverable Parameter command Sequence Diagram (ADS=0)

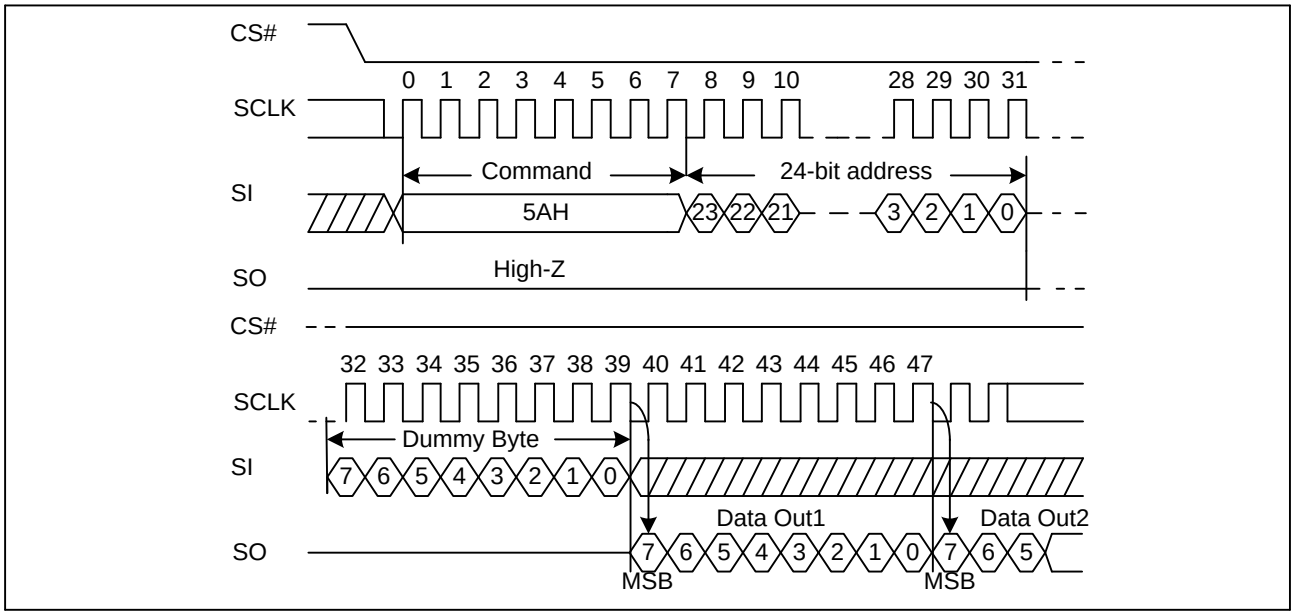


Figure 70 Read Serial Flash Discoverable Parameter command Sequence Diagram (ADS=1)

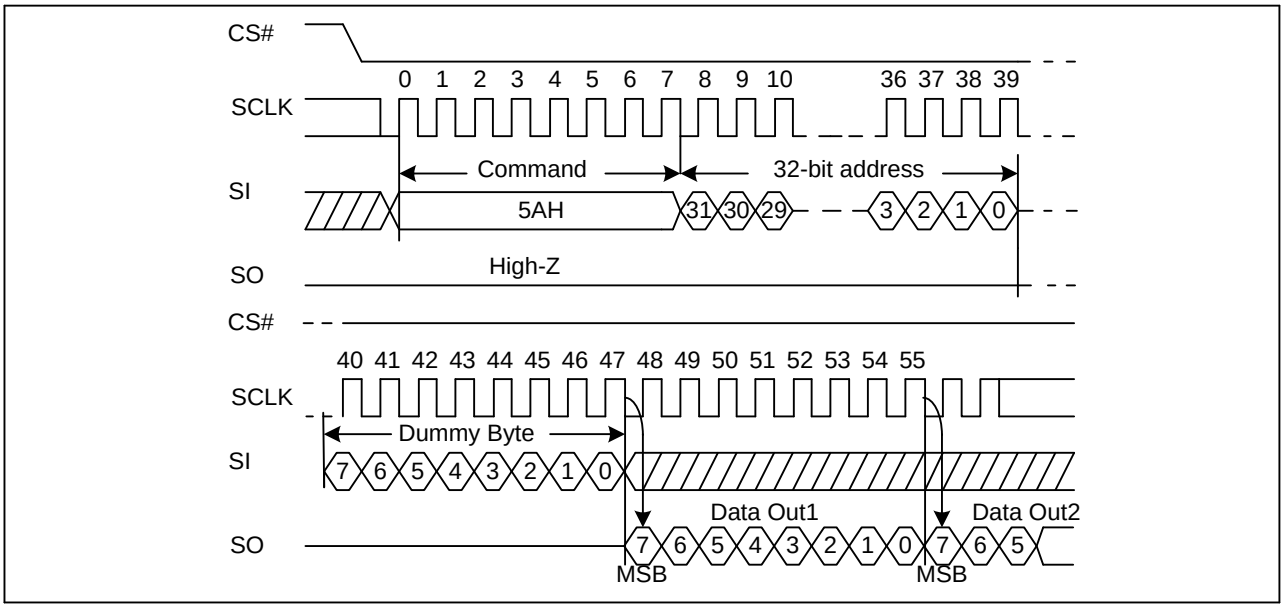


Table 21 Signature and Parameter Identification Data Values

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
SFDP Signature	Fixed:50444653H	00H	07:00	53H	53H
		01H	15:08	46H	46H
		02H	23:16	44H	44H
		03H	31:24	50H	50H
SFDP Minor Revision Number	Start from 00H	04H	07:00	00H	00H
SFDP Major Revision Number	Start from 01H	05H	15:08	01H	01H
Number of Parameters Headers	Start from 00H	06H	23:16	01H	01H
Unused	Contains 0xFFH and can never be changed	07H	31:24	FFH	FFH
ID number (JEDEC)	00H: It indicates a JEDEC specified header	08H	07:00	00H	00H
Parameter Table Minor Revision Number	Start from 0x00H	09H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	0AH	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0BH	31:24	09H	09H
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0CH	07:00	30H	30H
		0DH	15:08	00H	00H
		0EH	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	0FH	31:24	FFH	FFH
ID Number (GigaDevice Manufacturer ID)	It is indicates GigaDevice manufacturer ID	10H	07:00	C8H	C8H
Parameter Table Minor Revision Number	Start from 0x00H	11H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	12H	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13H	31:24	03H	03H
Parameter Table Pointer (PTP)	First address of GigaDevice Flash Parameter table	14H	07:00	60H	60H
		15H	15:08	00H	00H
		16H	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	17H	31:24	FFH	FFH

Table 22 Parameter Table (0): JEDEC Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Block/Sector Erase Size	00: Reserved; 01: 4KB erase; 10: Reserved; 11: not support 4KB erase	30H	01:00	01b	E5H
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Requested for Writing to Volatile Status Registers	0: Nonvolatile status bit 1: Volatile status bit (BP status register bit)		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50H Opcode, 1: Use 06H Opcode, Note: If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31H	15:08	20H	20H
(1-1-2) Fast Read	0=Not support, 1=Support	32H	16	1b	F3H
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	01b	
Double Transfer Rate (DTR) clocking	0=Not support, 1=Support		19	0b	
(1-2-2) Fast Read	0=Not support, 1=Support		20	1b	
(1-4-4) Fast Read	0=Not support, 1=Support		21	1b	
(1-1-4) Fast Read	0=Not support, 1=Support		22	1b	
Unused			23	1b	
Unused		33H	31:24	FFH	FFH
Flash Memory Density		37H:34H	31:00	0FFFFFFFH	
(1-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	38H	04:00	00100b	44H
(1-4-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		07:05	010b	
(1-4-4) Fast Read Opcode		39H	15:08	EBH	EBH
(1-1-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3AH	20:16	01000b	08H
(1-1-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		23:21	000b	
(1-1-4) Fast Read Opcode		3BH	31:24	6BH	6BH

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
(1-1-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3CH	04:00	01000b	08H
(1-1-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		07:05	000b	
(1-1-2) Fast Read Opcode		3DH	15:08	3BH	3BH
(1-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3EH	20:16	00010b	42H
(1-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	010b	
(1-2-2) Fast Read Opcode		3FH	31:24	BBH	BBH
(2-2-2) Fast Read	0=not support 1=support	40H	00	0b	EEH
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	0b	
Unused			07:05	111b	
Unused		43H:41H	31:08	0xFFH	0xFFH
Unused		45H:44H	15:00	0xFFH	0xFFH
(2-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	46H	20:16	00000b	00H
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47H	31:24	FFH	FFH
Unused		49H:48H	15:00	0xFFH	0xFFH
(4-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	4AH	20:16	00000b	00H
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(4-4-4) Fast Read Opcode		4BH	31:24	FFH	FFH
Sector Type 1 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	4CH	07:00	0CH	0CH
Sector Type 1 erase Opcode		4DH	15:08	20H	20H
Sector Type 2 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	4EH	23:16	0FH	0FH
Sector Type 2 erase Opcode		4FH	31:24	52H	52H
Sector Type 3 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	50H	07:00	10H	10H
Sector Type 3 erase Opcode		51H	15:08	D8H	D8H
Sector Type 4 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	52H	23:16	00H	00H
Sector Type 4 erase Opcode		53H	31:24	FFH	FFH

Table 23 Parameter Table (1): GigaDevice Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Vcc Supply Maximum Voltage	2000H=2.000V 2700H=2.700V 3600H=3.600V	61H:60H	15:00	3600H	3600H
Vcc Supply Minimum Voltage	1650H=1.650V 2250H=2.250V 2350H=2.350V 2700H=2.700V	63H:62H	31:16	2700H	2700H
HW Reset# pin	0=not support 1=support	65H:64H	00	1b	F99FH
HW Hold# pin	0=not support 1=support		01	1b	
Deep Power Down Mode	0=not support 1=support		02	1b	
SW Reset	0=not support 1=support		03	1b	
SW Reset Opcode	Should be issue Reset Enable(66H) before Reset cmd.		11:04	1001 1001b (99H)	
Program Suspend/Resume	0=not support 1=support		12	1b	
Erase Suspend/Resume	0=not support 1=support		13	1b	
Unused			14	1b	
Wrap-Around Read mode	0=not support 1=support		15	1b	
Wrap-Around Read mode Opcode		66H	23:16	77H	77H
Wrap-Around Read data length	08H:support 8B wrap-around read 16H:8B&16B 32H:8B&16B&32B 64H:8B&16B&32B&64B	67H	31:24	64H	64H
Individual block lock	0=not support 1=support	6BH:68H	00	1b	C78FH
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	1b	
Individual block lock Opcode			09:02	E3H	
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect		10	1b	
Secured OTP	0=not support 1=support		11	0b	
Read Lock	0=not support 1=support		12	0b	
Permanent Lock	0=not support 1=support		13	0b	
Unused			15:14	11b	
Unused			31:16	FFH	FFH

8. ELECTRICAL CHARACTERISTICS

8.1. POWER-ON TIMING

Figure 71 Power-on Timing

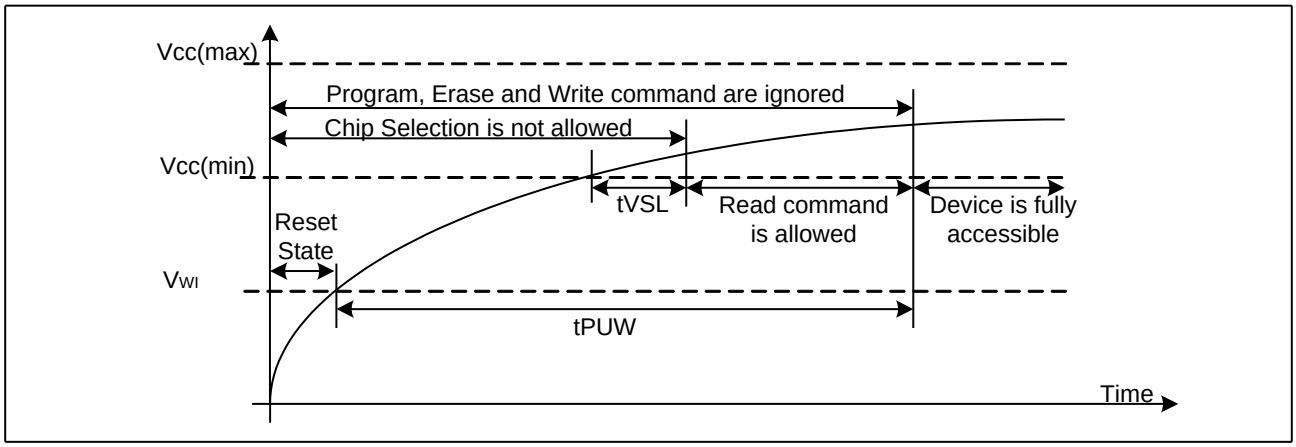


Table 24 Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min	Max	Unit
tVSL	VCC(min) To CS# Low	10		us
tPUW	Time Delay Before Write Instruction	1	10	ms
VWI	Write Inhibit Voltage	1	2.5	V

8.2. INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH). The Status Register bits are set to 0, except DRV1 bit (S9) is set to 1.

8.3. DATA RETENTION AND ENDURANCE

Table 25 Data Retention and Endurance

Parameter	Test Condition	Min	Units
Minimum Pattern Data Retention Time	150℃	10	Years
	125℃	20	Years
Erase/Program Endurance	-40 to 85℃	100K	Cycles

8.4. LATCH UP CHARACTERISTICS

Table 26 Latch up Characteristics

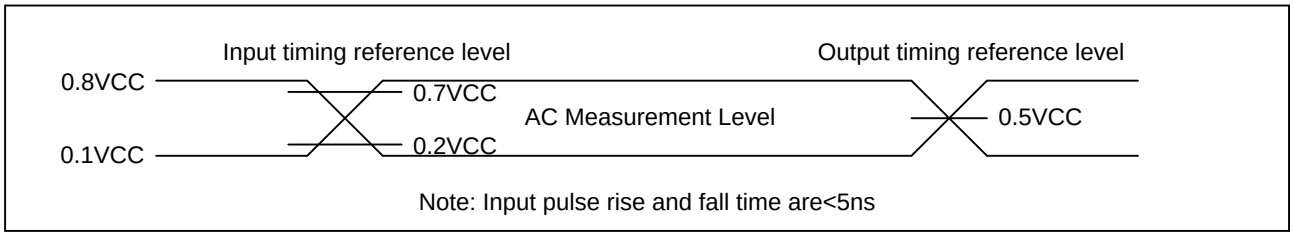
Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

8.5. ABSOLUTE MAXIMUM RATINGS

Table 27 Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-65 to 150	℃
Output Short Circuit Current	200	mA
Applied Input/Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V

Figure 72 Input/Output Timing Reference Level



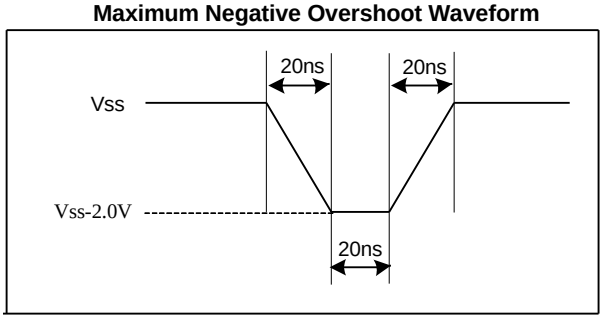
8.6. CAPACITANCE MEASUREMENT CONDITIONS

Table 28 Capacitance Measurement Conditions

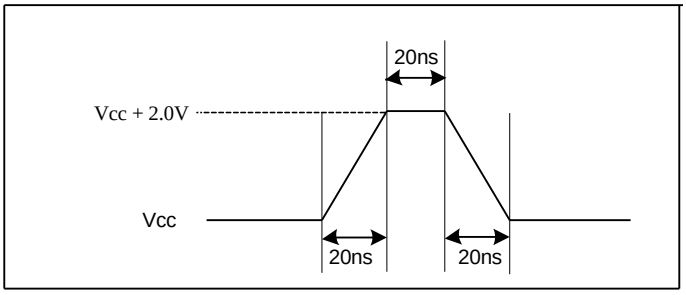
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Figure 73 Input Test Waveform and Measurement Level

Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform



8.7. DC CHARACTERISTICS

Table 29 DC CHARACTERISTICS (T= -40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS		60	200	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, V_{IN}=VCC or VSS		2	10	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 104MHz, Q=Open(*1,*2,*4 I/O)		15	20	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)		13	18	mA
I_{CC4}	Operating Current (PP)	CS#=VCC			20	mA
I_{CC5}	Operating Current(WRSR)	CS#=VCC			20	mA
I_{CC6}	Operating Current (SE)	CS#=VCC			20	mA
I_{CC7}	Operating Current (BE)	CS#=VCC			20	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} =100uA			0.2	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.2			V

Note:

1. Not 100% tested in production.

2.Tested on sample basis and specified through design and characterization data. T=25℃, VCC=3.0V.

8.8. AC CHARACTERISTICS

Table 30 AC CHARACTERISTICS (T= -40℃~85℃, VCC=2.7~3.6V, CL=30pf)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_C	Serial Clock Frequency for All Instructions Except Read	DC.		104	MHz
f_{C1}	Serial Clock Frequency for Dual I/O (BBH, BCH), Quad I/O (EBH, ECH), Dual Output(3BH, 3CH), Quad Output(6BH, 6CH), Fast Read (0BH, 0CH) Instructions, on 3.0 - 3.6V power supply	DC.		104	MHz
f_{C2}	Serial Clock Frequency for Dual I/O (BBH, BCH), Quad I/O (EBH, ECH), Dual Output(3BH, 3CH), Quad Output(6BH, 6CH), Fast Read (0BH, 0CH) Instructions, on 2.7 - 3.0V power supply	DC.		80	MHz
f_R	Serial Clock Frequency For: Read(03H, 13H)	DC.		80	MHz
t_{CLH}	Serial Clock High Time	3.7			ns
t_{CLL}	Serial Clock Low Time	3.7			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (read/write)	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	1.2			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{HLCH}	HOLD# Low Setup Time (relative to Clock)	5			ns
t_{HHCH}	HOLD# High Setup Time (relative to Clock)	5			ns
t_{CHHL}	HOLD# High Hold Time (relative to Clock)	5			ns
t_{CHHH}	HOLD# Low Hold Time (relative to Clock)	5			ns
t_{HLQZ}	HOLD# Low To High-Z Output			6	ns
t_{HHQX}	HOLD# Low To Low-Z Output			8	ns
t_{CLQV}	Clock Low To Output Valid			7	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			20	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			30	μs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			30	μs
t_{SUS}	CS# High To Next Command After Suspend			20	us
t_{RST}	CS# High To Next Command After Reset			60	us
t_W	Write Status Register Cycle Time		5	30	ms

t_{BP1}	Byte Program Time(First Byte)		30	50	us
t_{BP2}	Additional Byte Program Time (After First Byte)		2.5	12	us
t_{PP}	Page Programming Time		0.6	2.4	ms
t_{SE}	Sector Erase Time		50	300	ms
t_{BE}	Block Erase Time(32K Bytes)		0.2	1.0	s
t_{BE}	Block Erase Time(64K Bytes)		0.3	1.2	s
t_{CE}	Chip Erase Time(GD25Q512MC)		180	400	s

Note:

1. Not 100% tested in production.
2. Tested on sample basis and specified through design and characterization data. T=25℃, VCC=3.0V.

Figure 74 Serial Input Timing

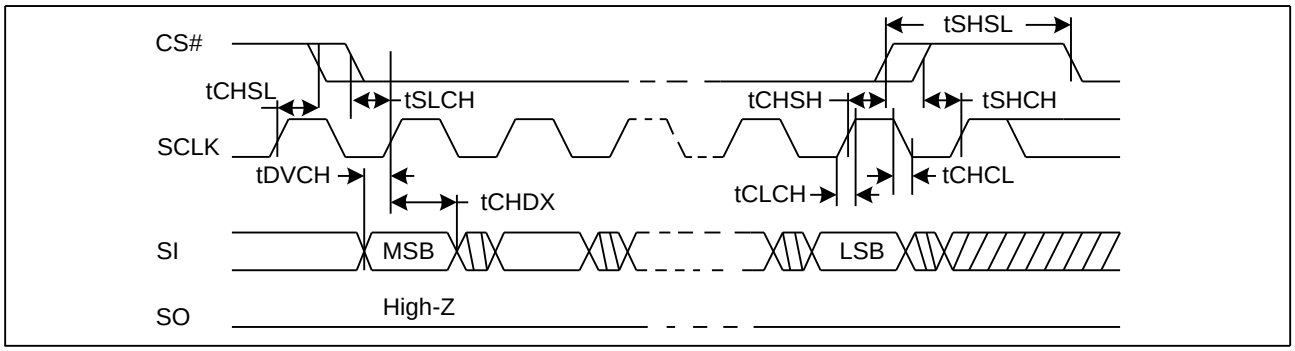


Figure 75 Output Timing

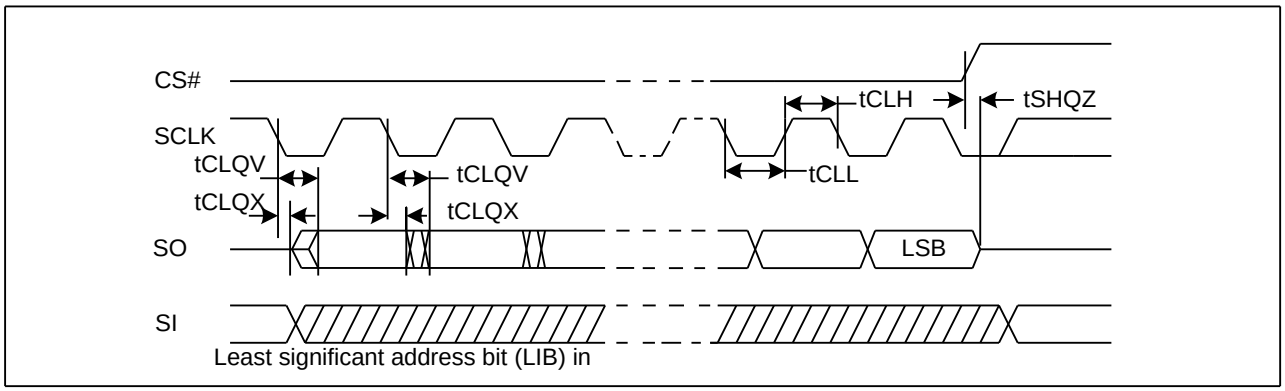


Figure 76 Hold Timing

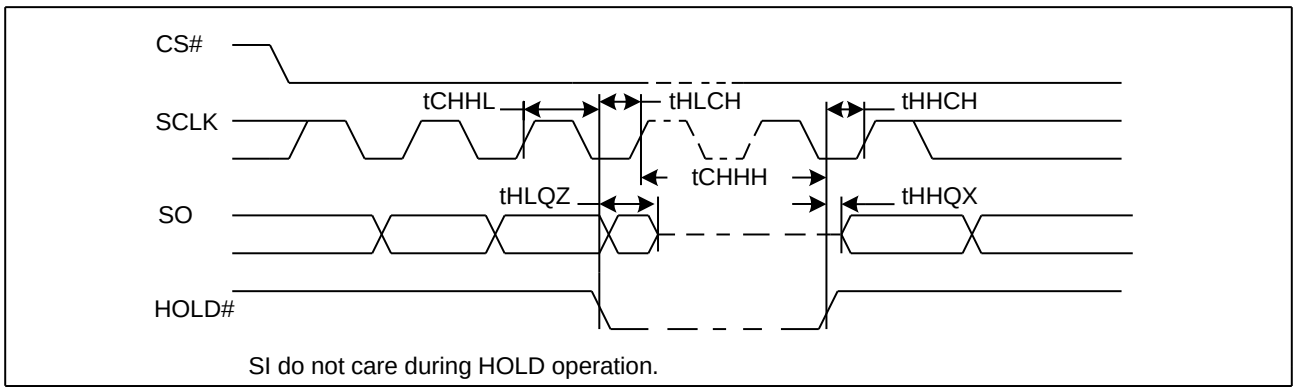


Figure 77 RESET Timing

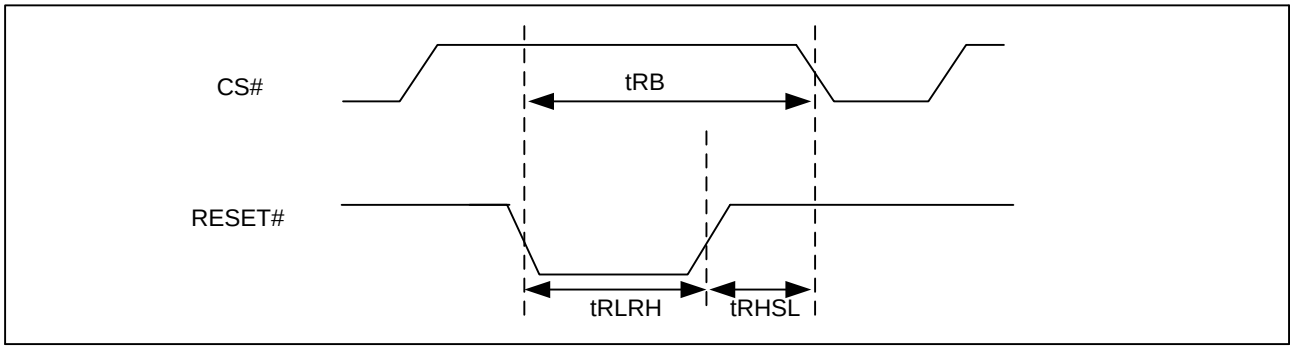
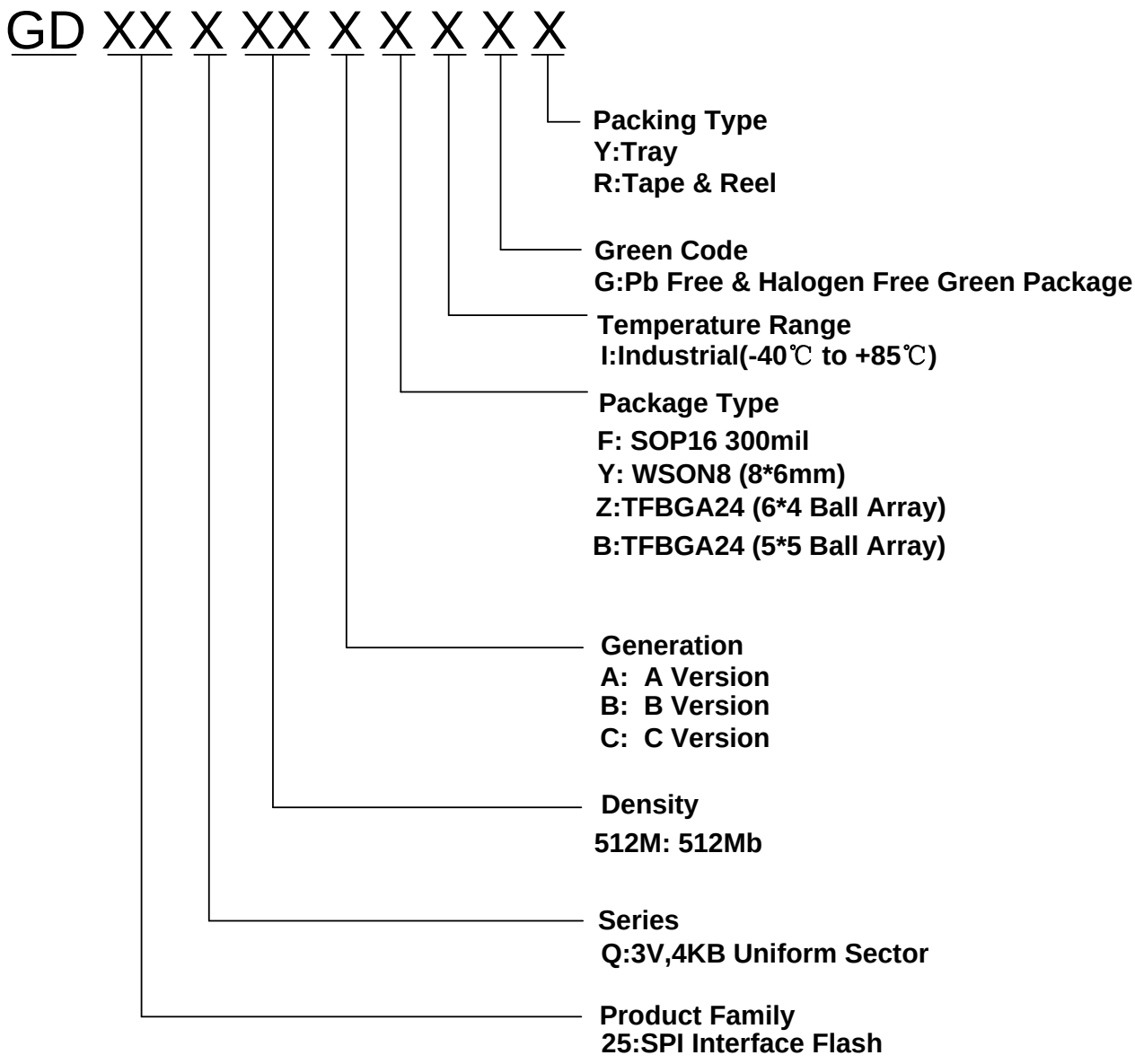


Table 31 Reset Timing

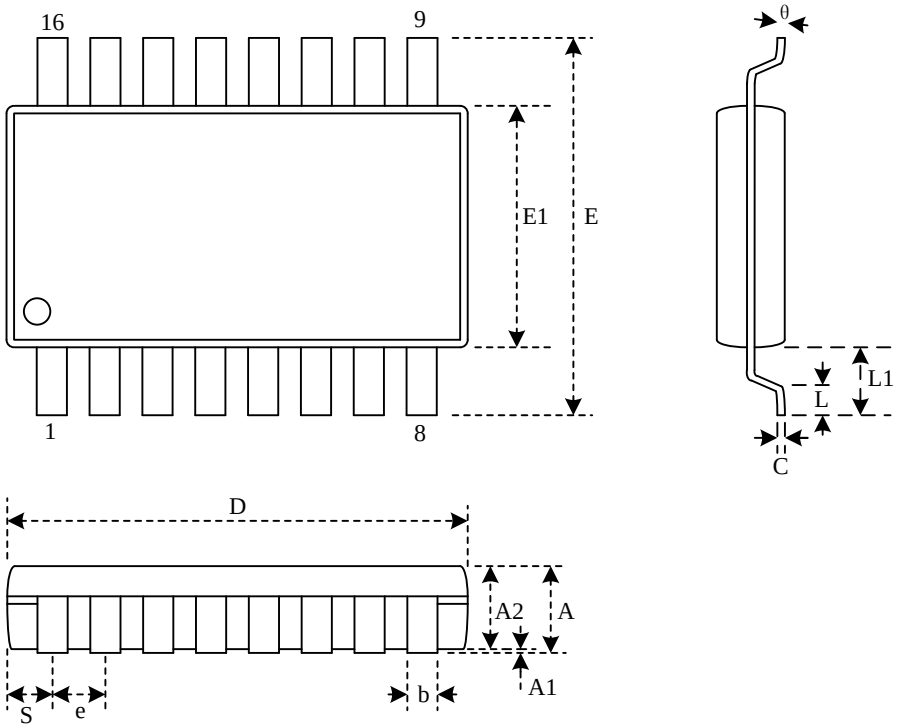
Symbol	Parameter	Setup	Speed	Unit.
tRLRH	Reset pulse width	MIN	1	us
tRHSL	Reset high time before read	MIN	50	ns
tRB	Reset recovery time	MAX	60	us

9. ORDERING INFORMATION



10. PACKAGE INFORMATION

10.1. Package SOP16 300MIL



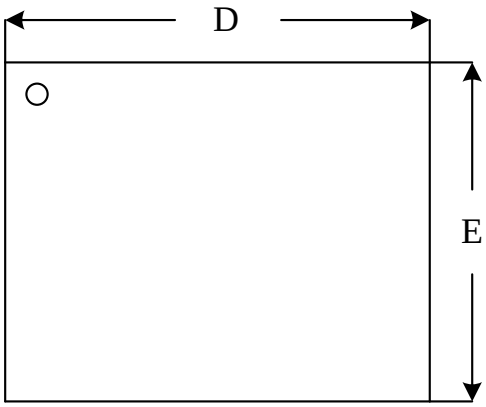
Dimensions

Symbol / Unit		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min	2.36	0.10	2.24	0.36	0.20	10.10	10.10	7.42		0.40	1.31	0.51	0
	Nom	2.55	0.20	2.34	0.41	0.25	10.30	10.35	7.52	1.27	0.84	1.44	0.64	5
	Max	2.75	0.30	2.44	0.51	0.30	10.50	10.60	7.60		1.27	1.57	0.77	8
Inch	Min	0.093	0.004	0.088	0.014	0.008	0.397	0.397	0.292		0.016	0.052	0.020	0
	Nom	0.100	0.008	0.092	0.016	0.010	0.405	0.407	0.296	0.050	0.033	0.057	0.025	5
	Max	0.108	0.012	0.096	0.020	0.012	0.413	0.417	0.299		0.050	0.062	0.030	8

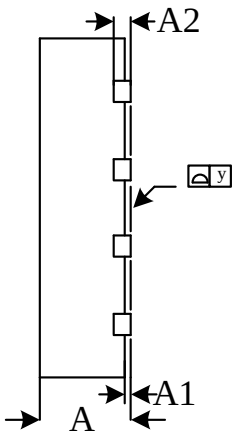
Note：Both package length and width do not include mold flash.

10.2. Package

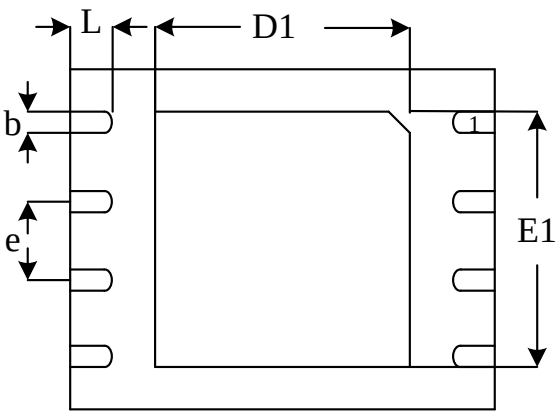
WSON 8 (8*6mm)



Top View



Side View



Bottom View

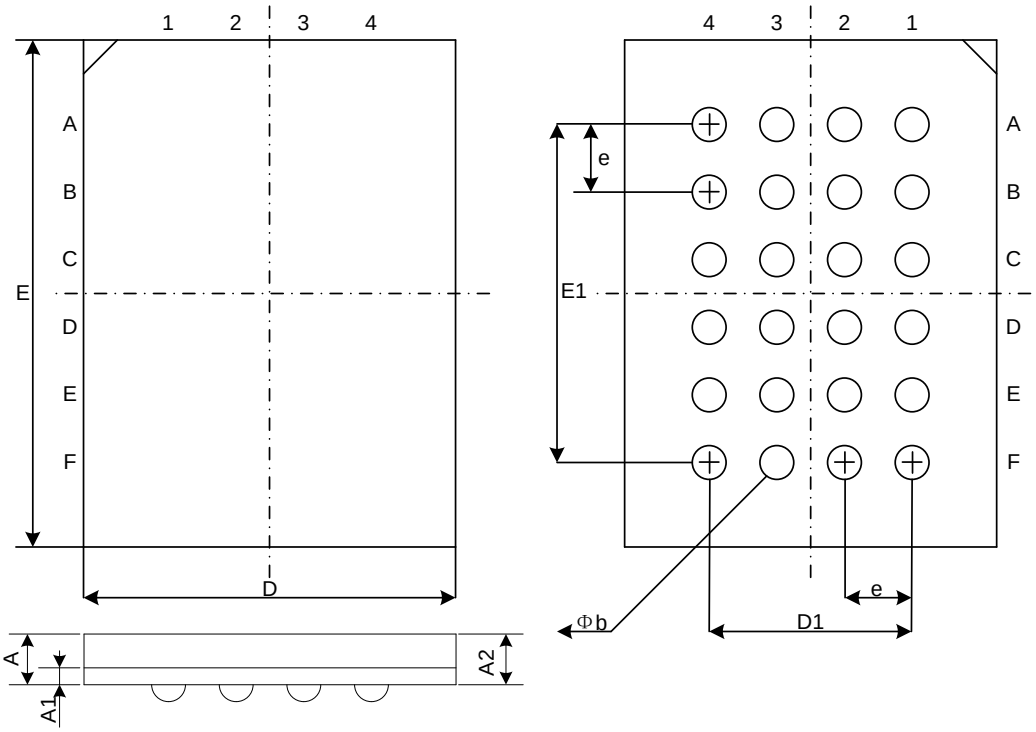
Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	K	L
mm	Min	0.70			0.35	7.90	3.25	5.90	4.15			0.55
	Nom	0.75		0.20BSC	0.40	8.00	3.42	6.00	4.30	1.27BSC	1.80	0.60
	Max	0.80	0.05		0.45	8.10	3.50	6.10	4.40			0.65
Inch	Min	0.028			0.014	0.311	0.128	0.232	0.163			0.022
	Nom	0.030		0.008BSC	0.016	0.315	0.135	0.236	0.169	0.050BSC	0.071	0.024
	Max	0.031	0.002		0.018	0.319	0.138	0.240	0.173			0.027

Note:

1. Both package length and width do not include mold flash.
2. The exposed metal pad area on the bottom of the package is connected to device ground (GND pin), so both Floating and connecting GND of exposed pad are also available.

10.3. Package TFBGA-24BALL (6*4 ball array)

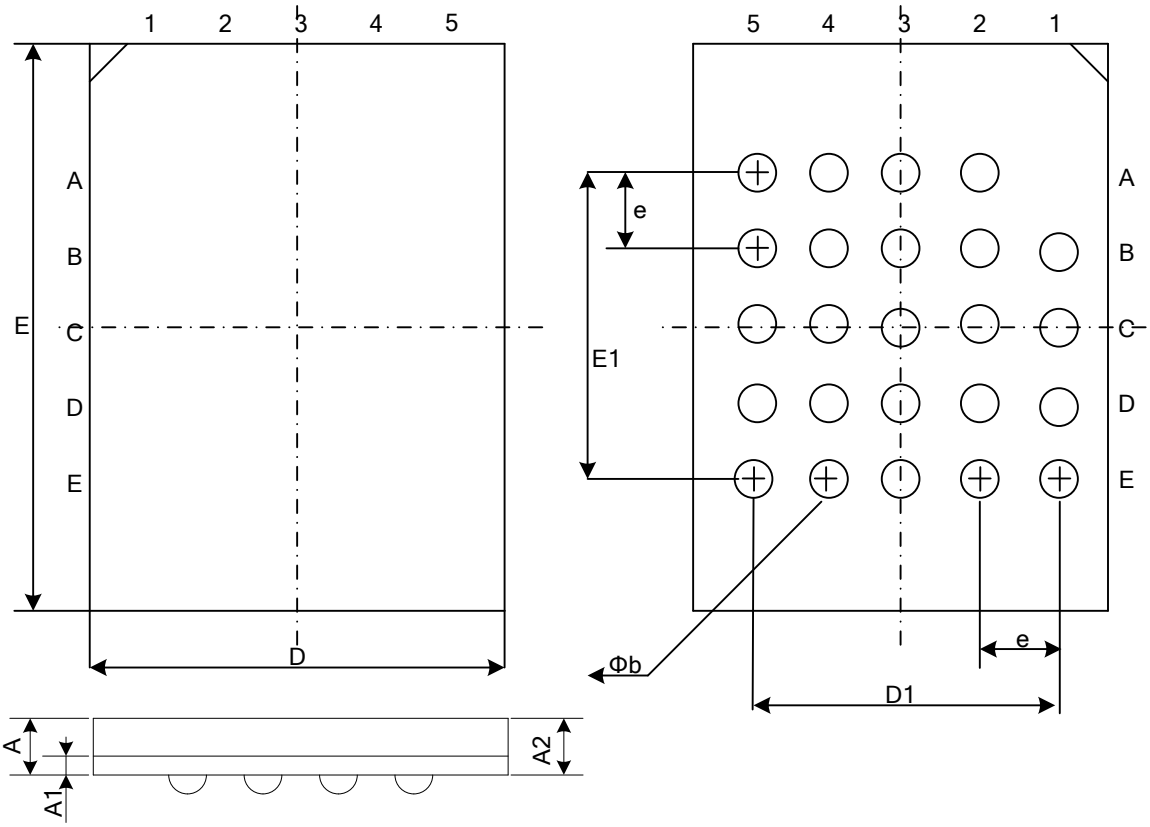


Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e
mm	Min		0.25		0.35	5.90		7.90		
	Nom		0.30	0.85	0.40	6.00	3.00	8.00	5.00	1.00
	Max	1.20	0.35		0.45	6.10		8.10		
Inch	Min		0.010		0.014	0.232		0.311		
	Nom		0.012	0.033	0.016	0.236	0.120	0.315	0.200	0.039
	Max	0.047	0.014		0.018	0.240		0.319		

Note：Both package length and width do not include mold flash.

10.4. Package TFBGA-24BALL (5*5 ball array)



Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e
mm	Min		0.25		0.35	5.90		7.90		
	Nom		0.30		0.40	6.00	4.00	8.00	4.00	1.00
	Max	1.20	0.35		0.45	6.10		8.10		
Inch	Min		0.010	0.033	0.014	0.232		0.311		
	Nom		0.012		0.016	0.236	0.157	0.315	0.157	0.039
	Max	0.047	0.014		0.018	0.240		0.319		

Note：Both package length and width do not include mold flash.

11. REVISION HISTORY

Version No	Description	Date
0.0	Initial Preliminary Release	2014/6/26
0.1	Modify Package WSON8 8x6mm	2014/8/4
0.2	Modify Command Description table number	2014/9/19
0.3	Add OTP description and command 42H, 44H, 48H Add Read Manufacturer ID/device ID(90H) and Read Identification(ABH) Modify DC CHARACTERISTICS:Icc4~7 max 10mA change to 20mA Modify DC CHARACTERISTICS: V_{IL} max 0.3Vcc change to 0.2Vcc Modify AC CHARACTERISTICS: tHHQX max 6us change to 8us Modify AC CHARACTERISTICS: tCE typ 80s/160s change to 100s/180s Modify Unique ID length to 8 byte Modify AC CHARACTERISTICS: tRB1 and tRB2 combine to tRB max 60us Modify Input/Output Timing Reference Level Modify Latency Code and Frequency Table Add note on DC/AC Characteristics Table and Latency Code and Frequency Table	2014-11-4
0.4	Modify Package TFBGA-24BALL (6*4 ball array) Modify Package TFBGA-24BALL (5*5 ball array)	2015-7-23